Multi-Chip Package MEMORY
256M Bit(32Mx8) Nand Flash / 512M Bit (8Mx16x4Banks) DDR2 SDRAM

Revision No.	History	Draft Date	Remark
Rev00	Initial Draft	Dec, 2009	Preliminary
Rev01	Modified Ordering Information	Jun, 2011	

MCP Product list

Part number	NAND product	DDR2 SDRAM	Package
MST7A08D16DMFC-XXX	256 Mbit(x8) – 3.3V	512 Mbit(x16) – 1.8V	FBGA 104 ball

Multi-Chip Package MEMORY

256M Bit (32Mx8) NAND Flash / 512M Bit (8Mx16x4Banks) DDR2 SDRAM

<MCP Features>

. Operating Temperature : 0℃ ~ 70℃
. 104-ball FBGA Type -9.0mmx9.0mm,0.65mm pitch

<NAND Features>

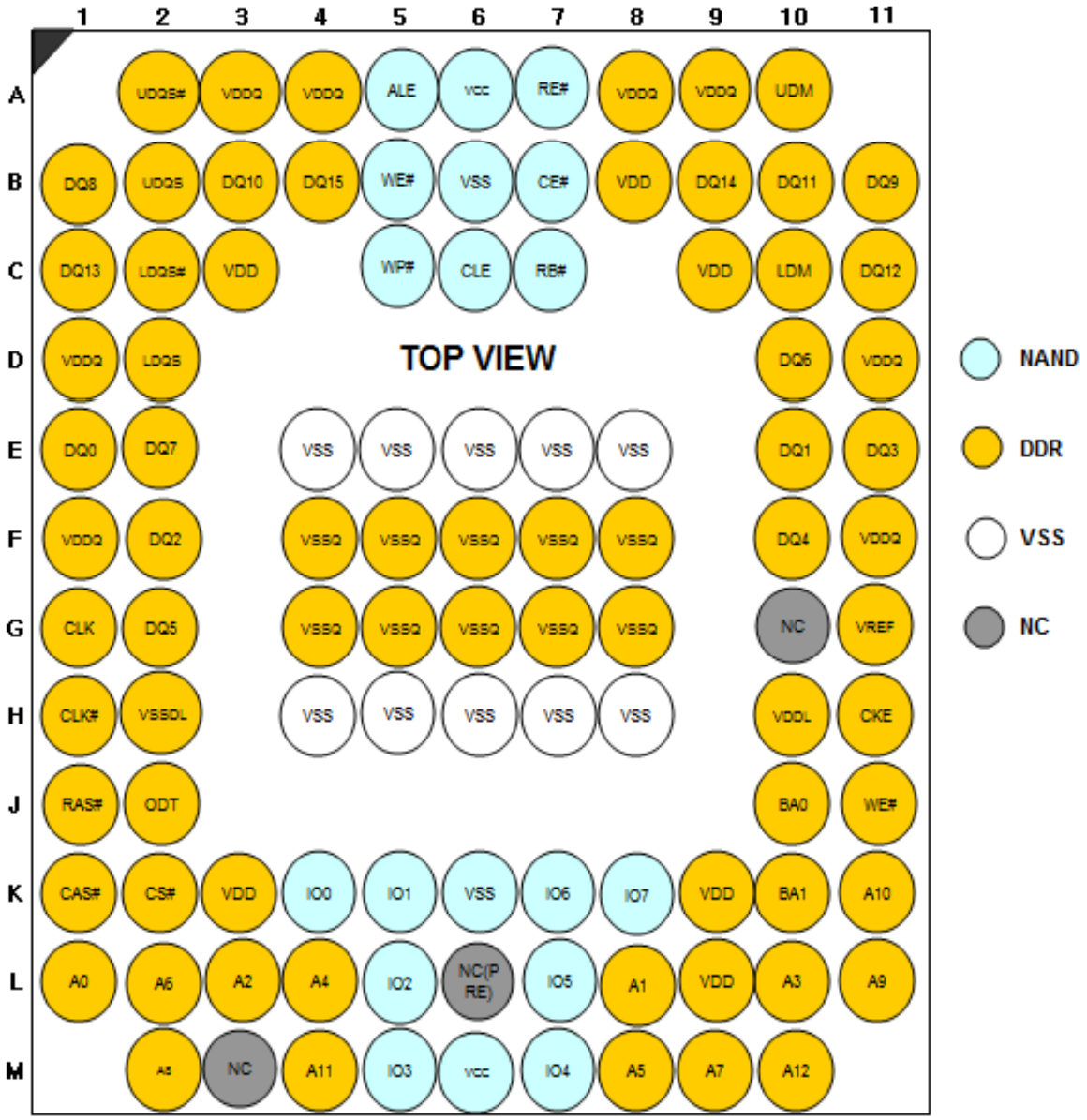
. Power Supply Voltage : 2.7~3.6V
. Organization
 - Memory Cell Array : (32M + 1024K)bit x 8 bit
. Data Register : (512 + 16)bit x 8bit
. Automatic Program and Erase
 - Page Program : (512 + 16)Byte
 - Block Erase : (16K + 512)Byte
. Page Read Operation
 - Page Size : (512 + 16)Byte
 - Random Access : 12μs(Max.)
 - Serial Page Access : 50ns(Min.)
. Fast Write Cycle Time
 - Program time : 200μs(Typ.)
 - Block Erase Time : 2ms(Typ.)
. Command/Address/Data Multiplexed I/O Port
. Hardware Data Protection
 - Program/Erase Lockout During Power Transitions
. Data Integrity
 - Endurance : 100K Program/Erase Cycles
 - Data Retention : 10 Years
. Command Register Operation

<DDR2 SDR Features>

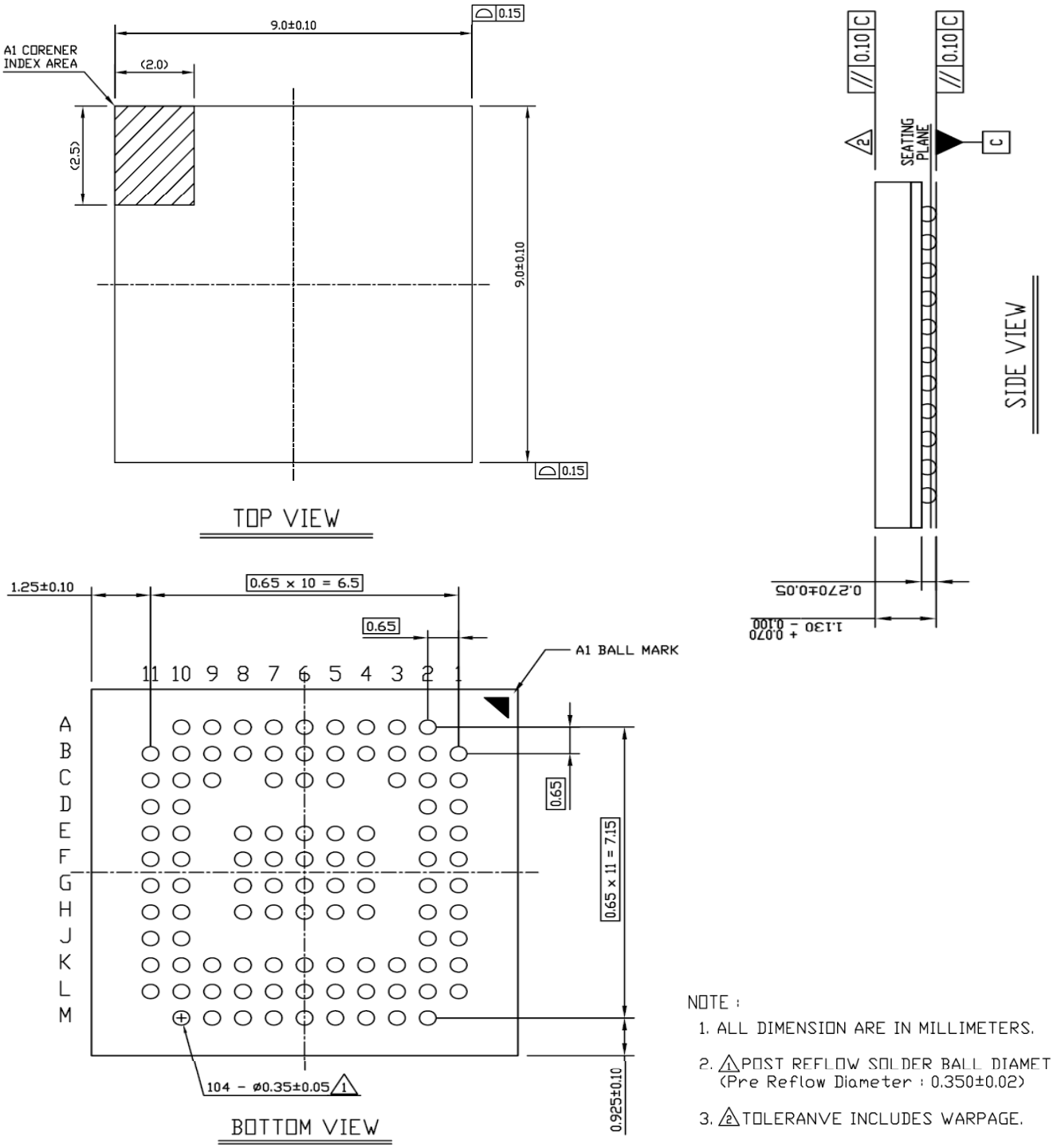
. Density: 512M bits
. Organization
 - 8M words × 16 bits × 4 banks
. Power supply: 1.8V ± 0.1V
. Data rate:800Mbps/667Mbps/
 533Mbps/400Mbps
. Four internal banks for concurrent operation
. Interface: SSTL_18
. Burst lengths (BL): 4, 8
. Burst type (BT):
 - Sequential (4, 8)
 - Interleave (4, 8)
. /CAS Latency (CL): 3, 4, 5, 6
. Precharge: auto precharge option for each Burst access
. Driver strength: normal/weak
. Refresh: auto-refresh, self-refresh
. Refresh cycles: 8192 cycles/64ms
 - Average refresh period
 7.8μs at 0 ℃ ≤ TC ≤ +85 ℃
 3.9s at +85 ℃ < TC +95 ℃

MST7A08D16DMFC is a Multi Chip Package Memory which combines 256Mbit NAND Flash Memory and 512Mbit DDR2 Synchronous Dynamic RAM. 256MB NAND Flash Memory is organized as 32M x 8bits and 512MB DDR2 SDR is organized as 8M x 16bits x 4Banks. In 256Mbit NAND Flash, its NAND cell provides the most cost effective –solution for the solid state mass storage market. A program operation can be performed in typical 200μs on the 528-byte Page and an erase operation can be performed in typical 2ms on a 16K-byte block. Data in the page can be read out at 50ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write control automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. In 512Mbit DDR2 SDR, Synchronous design allows precise cycle control with the use of system clock and I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst lengths and programmable latencies allow the same device to be useful for a variety of high bandwidth and high performance memory system applications. MST7A08D16 DMFC is available in 104-ball FBGA Type.

PIN CONFIGURATION (9x9mm, 104-FBGA)



Package Drawing (9x9mm, 104-FBGA)



PIN DESCRIPTION -104-FBGA

Pin Name	Function (DDR SDRAM)
A0~A12	Address Inputs
BA0, BA1	Block Select Address
DQ0~DQ15	Data Input/Output
LDQS, UDQS	Input and Output Data Strobe
CS#	Chip Select
RAS#	Row Address Strobe Command
CAS#	Column Address Strobe Command
WEd#	Write Enable
LDM, UDM	Input Mask
CLK	Clock Input
CLK#	Differential Clock Input
CKE	Clock Enable
VREF	Input Reference Voltage
VDD	Power Supply
VDDQ	Power for DQ Circuit
VSSQ	Ground for DQ Circuit
ODT	On-Die Terminal Control

Pin Name	Function (NAND Flash)
IO0~IO7	Input and Output
CE#	Chip Enable
WEn#	Write Enable
RE#	Read Enable
ALE	Address Latch Enable
CLE	Command Latch Enable
WP#	Write Protect
R/B#	Ready/Busy
PRE	Power On-Read Enable, Lock Unlock
VCC	Power Supply

Pin Name	Function
Vss	Ground
NC	No Connection
DNU	Do Not Use

PART NUMBERING