Multi-Chip Package MEMORY
1G Bit(128Mx8) NAND Flash / 1G Bit (8Mx16x8Banks) DDR2 SDRAM

Revision No.	History	Draft Date	Remark
Rev 00	Initial Draft	Nov. 2010	Preliminary
Rev 01	1. Changed Operating Temperature at standard grade : From : 0℃ ~ 85℃ To : 0℃ ~ 95℃ (Refer to page 96) 2. Updated IDD parameter (Refer to Page 110)	Jun. 2011	

Multi-Chip Package MEMORY

1G Bit (128Mx8) NAND Flash / 1G Bit (8Mx16x8Banks) DDR2 SDRAM

<MCP Features>

- Operating Temperature : 0℃ ~ 85℃
- 119-ball FBGA Type - 10mm x 13mm, 0.8mm pitch
- 104-ball FBGA Type – 9.0mm x9.0mm, 0.65mm pitch

<NAND Features>

- **Power Supply Voltage**
  - 2.7V ~ 3.6V
- **Organization**
  - Memory Cell Array : (128M + 4M)bit x 8 bit
- **Data Register : (2048 + 64)bit x 8 bit**
- **Automatic Program and Erase**
  - Page Program : (2048 + 64)Byte
  - Block Erase : (128K + 4K)Byte
- **Page Read Operation**
  - Page Size : (2048 + 64)Byte
  - Random Access : 25μs (Max.)
  - Serial Page Access : 25ns(Min.)
- **Fast Write Cycle Time**
  - Program time : 200μs (Typ.)
  - Block Erase Time : 2ms(Typ.)
- **Command/Address/Data Multiplexed I/O Port**
- **Hardware Data Protection**
  - Program/Erase Lockout During Power Transitions
- **Data Integrity**
  - Endurance : 100K Program/Erase Cycles (with 1 bit / 528byte ECC)
  - Data Retention : 10 Years
- **Command Register Operation**

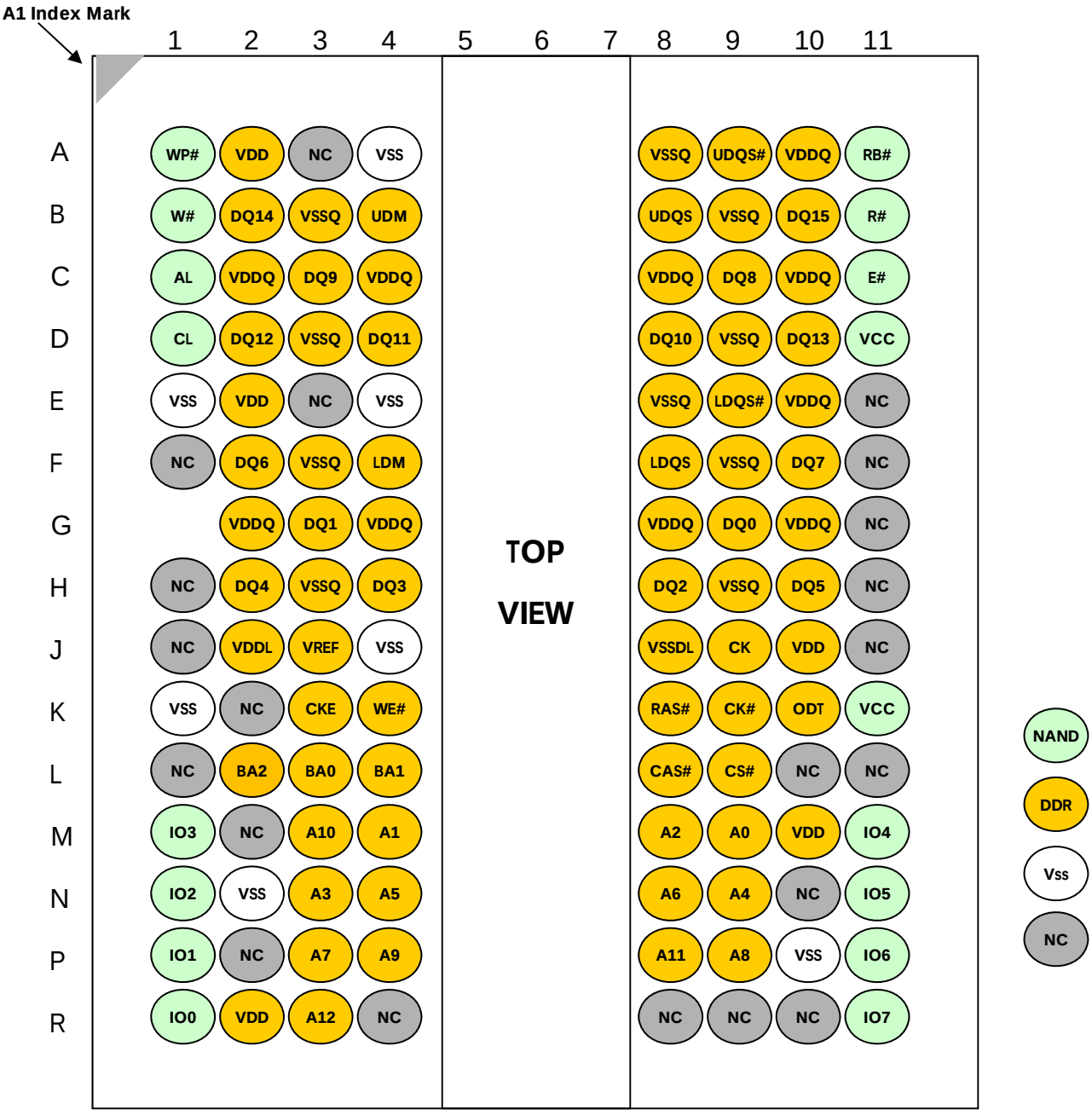
<DDR2 SDR Features>

- **Density:** 1G bits
- **Organization :** 8M × 16 bits × 8 banks
- **Power supply:**1.8V ± 0.1V
- **Data rate:** 667/800 (max.)
- **8 internal memory banks**
- **Programmable CAS Latency:**3,4,5
- **Programmable Additive Latency :** 0,1,2,3,4,5
- **Write Latency =** Read Latency -1
- **Programmable Burst Length :**
  4 and 8 Programmable Sequential / Interleave Burst
- **OCD (Off-chip Driver Impedance Adjustment)**
- **ODT (On-Die Termination)**
- **4n-bit prefetch architecture**
- **Data-Strobes :** Bidirectional, Differential
- **Auto-Refresh and Self-Refresh**
- **Strong and Weak Strength Data-Output Driver**
- **2KB Page Size**
- **7.8us max. Average Periodic Refresh Interval**

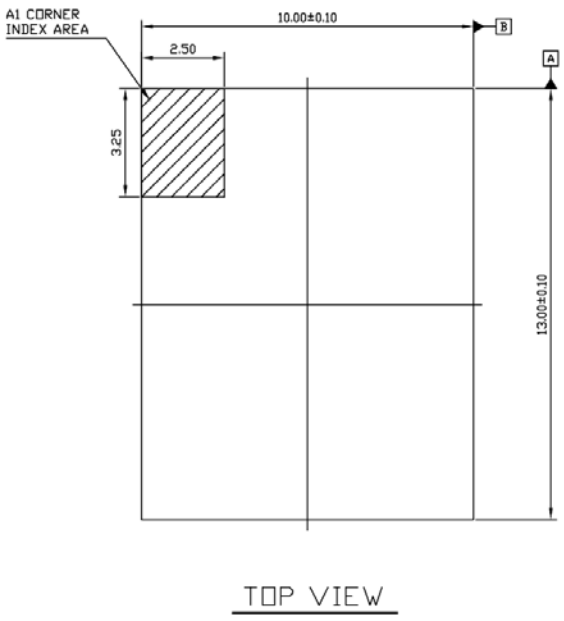
MCP Product Information

Part number	NAND Flash	DDR2 SDRAM	Package (FBGA)
MST7D08F16DMH-266	1G bit(x8) – 3.0V	1Gbit(x16) – 1.8V	10x13mm 119 ball
MST7D08F16DMHC-266	1G bit(x8) – 3.0V	1Gbit(x16) – 1.8V	9x9mm 104 ball

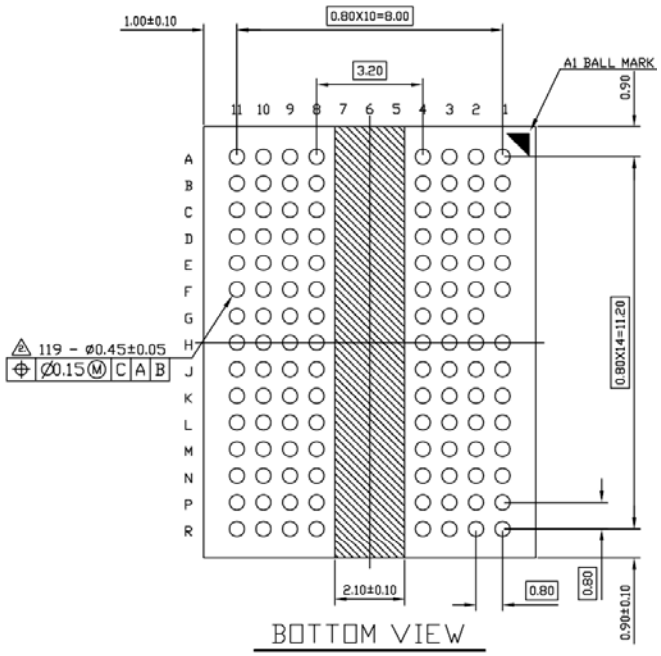
PIN CONFIGURATION(10.0x13.0mm, 119-FBGA)



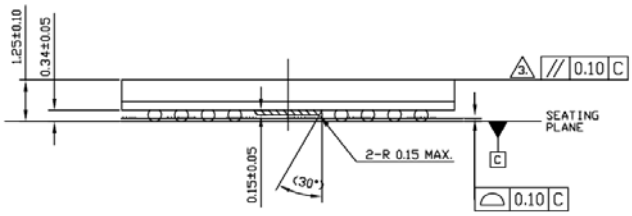
Package Drawing(10.0x13.0mm, 119-FBGA)



TOP VIEW



BOTTOM VIEW

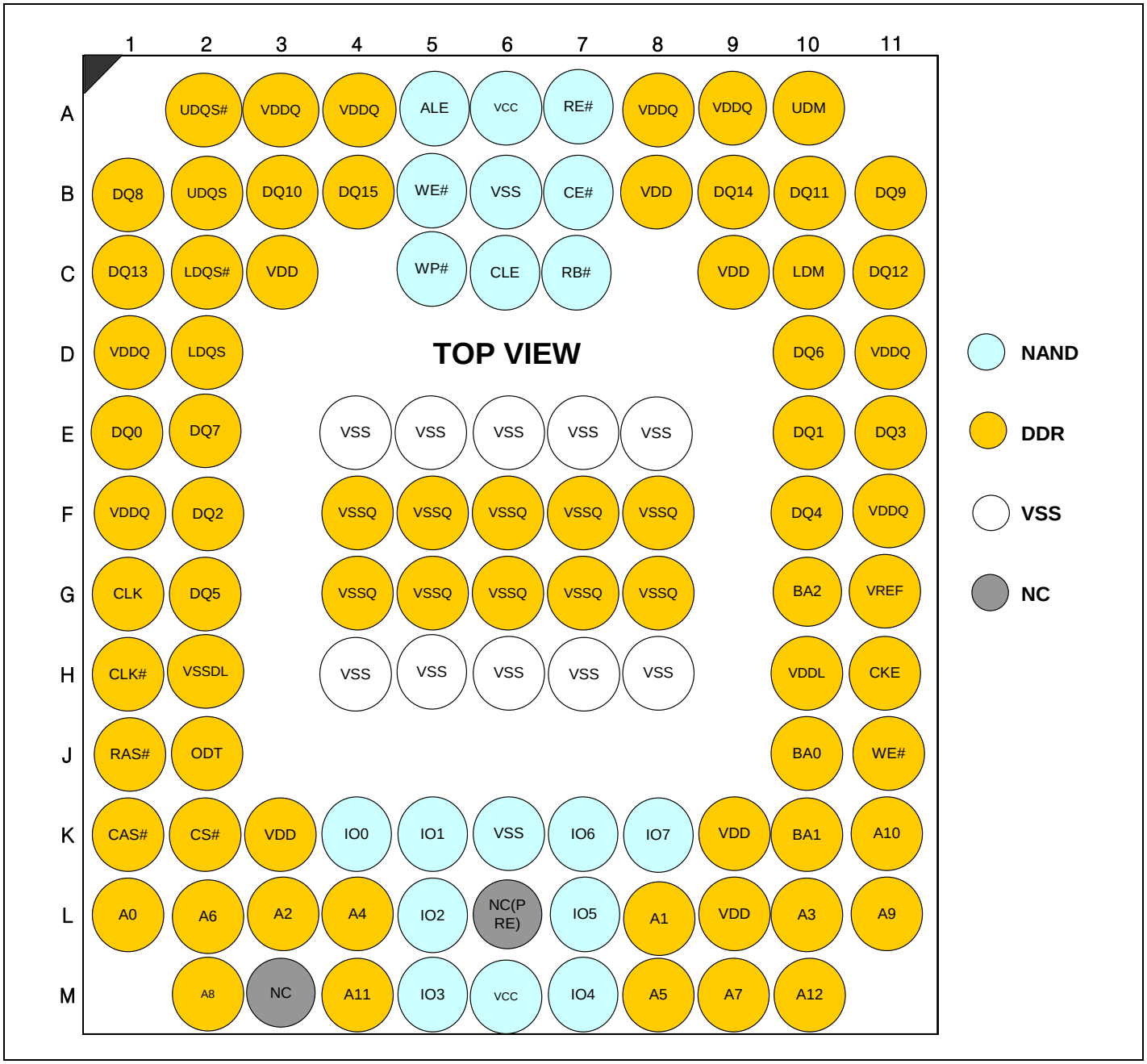


SIDE VIEW

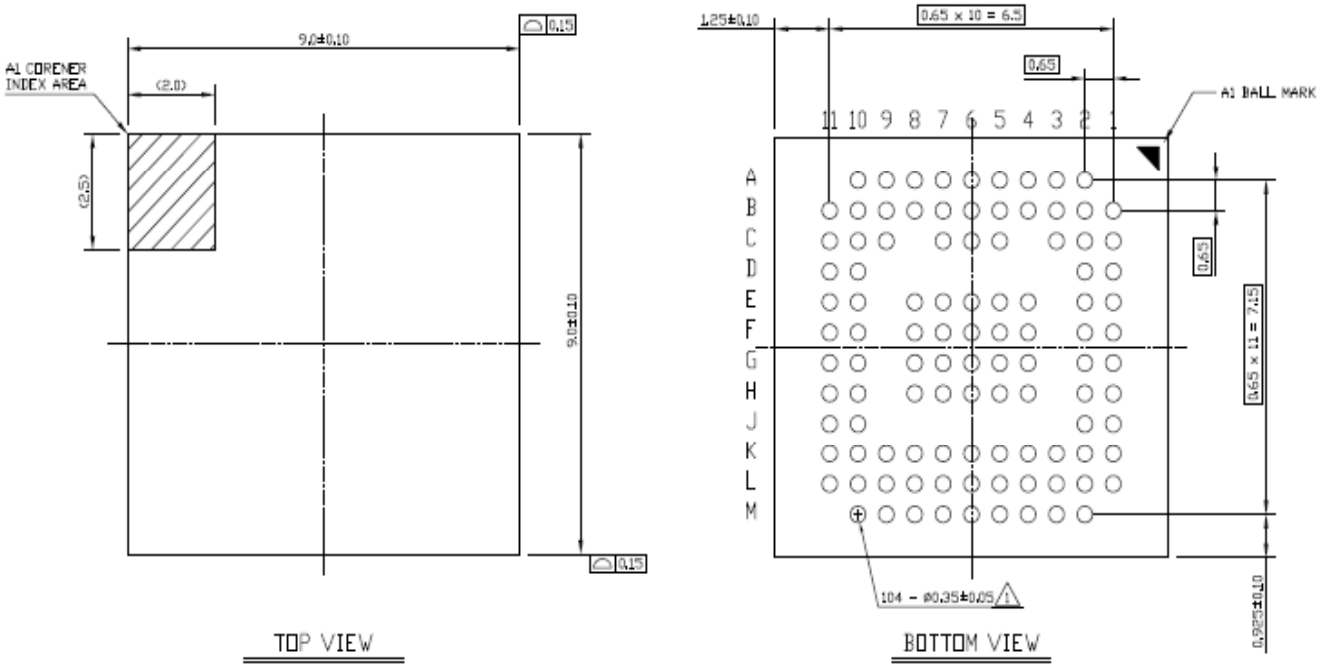
Description
FBGA 119BALL
Dimension
10.0mm x 13.0mm x 1.35mm

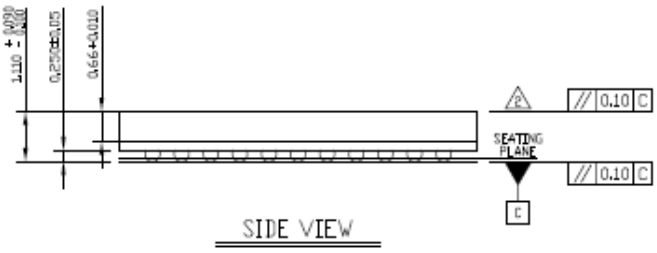
1. **ALL DIMENSIONS are in Millimeters.**
2. **POST REFLOW SOLDER BALL DIAMETER.**
   (Pre Reflow diameter : Ø0.45±0.02)
3. **TOLARENCE INCLUDES WARPAGE.**

PIN CONFIGURATION(9.0x9.0mm, 104-FBGA)



Package Drawing(9.0x9.0mm, 104-FBGA)





Description
FBGA 104BALL
Dimension
9.0mm x 9.0mm x 1.20mm

1. **ALL DIMENSIONS are in Millimeters.**
2. **POST REFLOW SOLDER BALL DIAMETER.**
   (Pre Reflow diameter : Ø0.35±0.02)
3. **TOLARENCE INCLUDES WARPAGE.**

PIN DESCRIPTION

Pin Name	Function (DDR2 SDRAM)
A0~A12	Address Inputs
BA0, BA1, BA2	Block Select Address
DQ0~DQ15	Data Input/Output
LDQS, $\overline{\text{LDQS}}$	Low Data Strobe
UDQS, $\overline{\text{UDQS}}$	Up Data Strobe
$\overline{\text{CS}}$	Chip Select
$\overline{\text{RAS}}$	Row Address Strobe Command
$\overline{\text{CAS}}$	Column Address Strobe Command
$\overline{\text{WE}}$	Write Enable
LDM, UDM	Input Mask
CLK	Clock Input
CLK#	Clock Input
CKE	Clock Enable
VREF	Input Reference Voltage
VDD	Power Supply
VDDQ	Power for DQ Circuit
VSSQ	Ground for DQ Circuit
VDDL	Power for DLL
VSSDL	Ground for DLL
ODT	On-Die Terminal Control

Pin Name	Function (NAND Flash)
IO0~IO7	Input and Output
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{WE}}$	Write Enable
$\overline{\text{RE}}$	Read Enable
ALE	Address Latch Enable
CLE	Command Latch Enable
$\overline{\text{WP}}$	Write Protect
R/$\overline{\text{B}}$	Ready/Busy
VCC	Power Supply

Pin Name	Function
VSS	Ground
NC	No Connection

Ordering Information