



1Gb NAND FLASH + 2Gb DDR2 SDRAM MCP Product

Multi-Chip Package MEMORY

1G Bit(128Mx8) NAND Flash / 2G Bit (16Mx16x8Banks) DDR2 SDRAM

Revision No.	History	Draft Date	Remark
Rev 00	Initial Draft	Sep. 2011	Preliminary
Rev 01	Adjust package thickness specification (From 1.35mm To 1.45mm (Max))	Nov. 2011	



Multi-Chip Package MEMORY

1G Bit (128Mx8) NAND Flash / 2G Bit (16Mx16x8Banks) DDR2 SDRAM

<MCP Features>

- Operating Temperature : 0°C ~ 85°C
- 119-ball FBGA Type - 10mm x 13mm, 0.8mm pitch

<NAND Features>

- **Power Supply Voltage**
 - 2.7V ~ 3.6V
- **Organization**
 - Memory Cell Array : (128M + 4M)bit x 8 bit
- **Data Register : (2048 + 64)bit x 8 bit**
- **Automatic Program and Erase**
 - Page Program : (2048 + 64)Byte
 - Block Erase : (128K + 4K)Byte
- **Page Read Operation**
 - Page Size : (2048 + 64)Byte
 - Random Access : 25μs (Max.)
 - Serial Page Access : 25ns(Min.)
- **Fast Write Cycle Time**
 - Program time : 200μs (Typ.)
 - Block Erase Time : 2ms(Typ.)
- **Command/Address/Data Multiplexed I/O Port**
- **Hardware Data Protection**
 - Program/Erase Lockout During Power Transitions
- **Data Integrity**
 - Endurance : 100K Program/Erase Cycles
(with 1 bit / 528byte ECC)
 - Data Retention : 10 Years
- **Command Register Operation**

<DDR2 SDR Features>

- **Density:** 2G bits
- **Organization :** 16M × 16 bits × 8 banks
- **Power supply:**1.8V ± 0.1V
- **Data rate:** 667/800 (max.)
- **8 internal memory banks**
- **Programmable CAS Latency:**3,4,5
- **Programmable Additive Latency :** 0,1,2,3,4,5
- **Write Latency =** Read Latency -1
- **Programmable Burst Length :**
 - 4 and 8 Programmable Sequential / Interleave Burst
- **OCD (Off-chip Driver Impedance Adjustment)**
- **ODT (On-Die Termination)**
- **4n-bit prefetch architecture**
- **Data-Strobes :** Bidirectional, Differential
- **Auto-Refresh and Self-Refresh**
- **Strong and Weak Strength Data-Output Driver**
- **2KB Page Size**
- **7.8us max. Average Periodic Refresh Interval**



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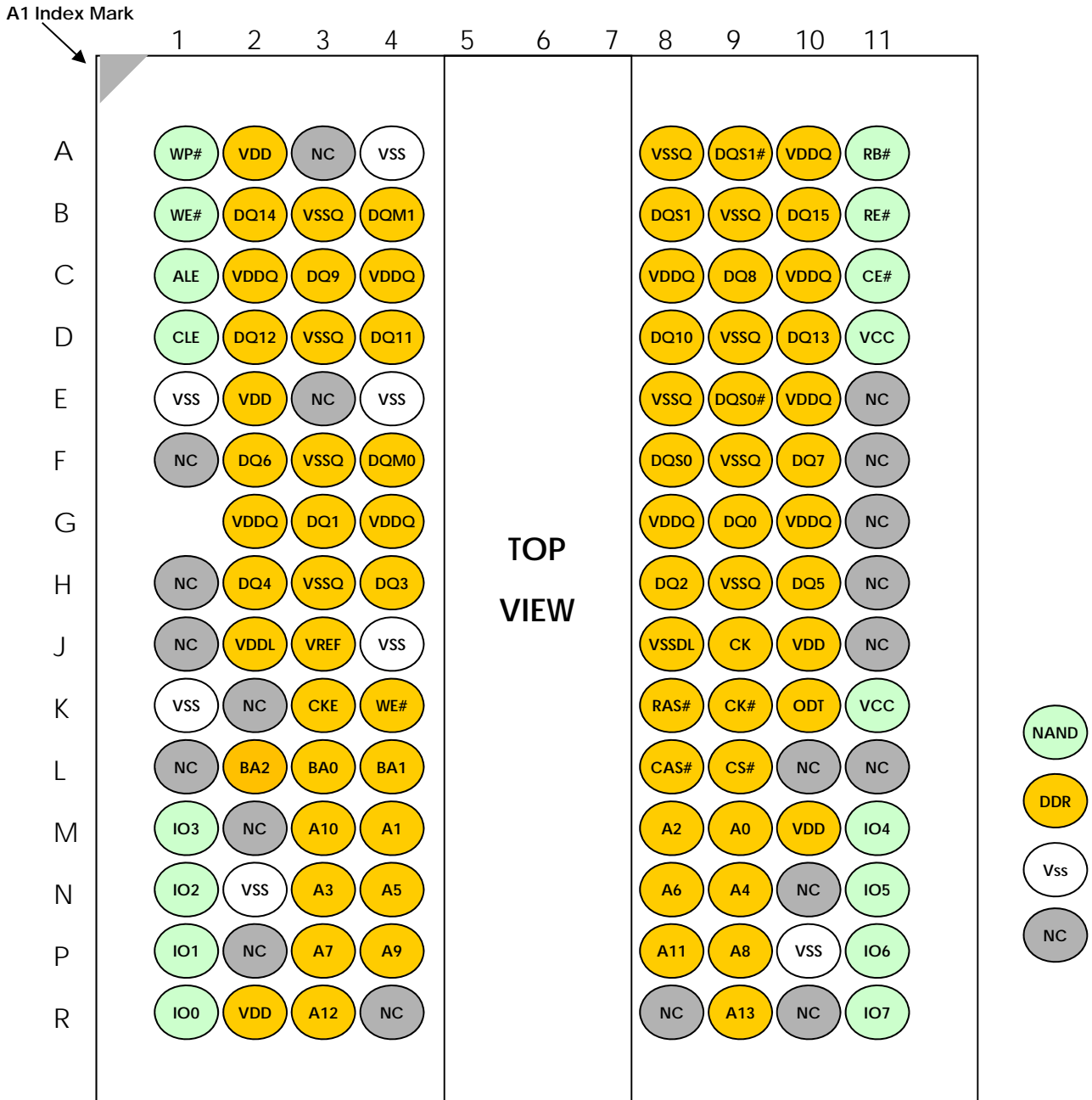
MCP Product Information

Part number	NAND Flash		DDR3 SDRAM		Package (FBGA)
	Density	Voltage	Density/Voltage	Speed	
MST7D08G16DMH-266	1G bit(x8)	2.7 - 3.6V	2Gbit(x16) / 1.8V	667Mbps	10x13mm 119 ball
MST7D08G16DMH-280	1G bit(x8)	2.7 - 3.6V	2Gbit(x16) / 1.8V	800Mbps	10x13mm 119 ball



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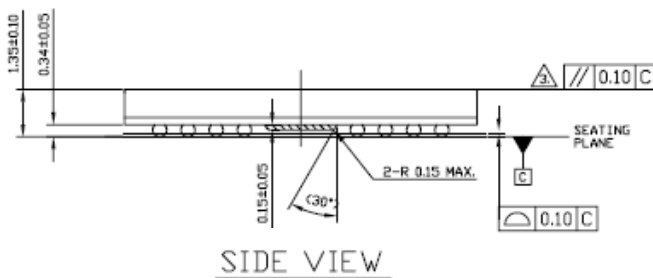
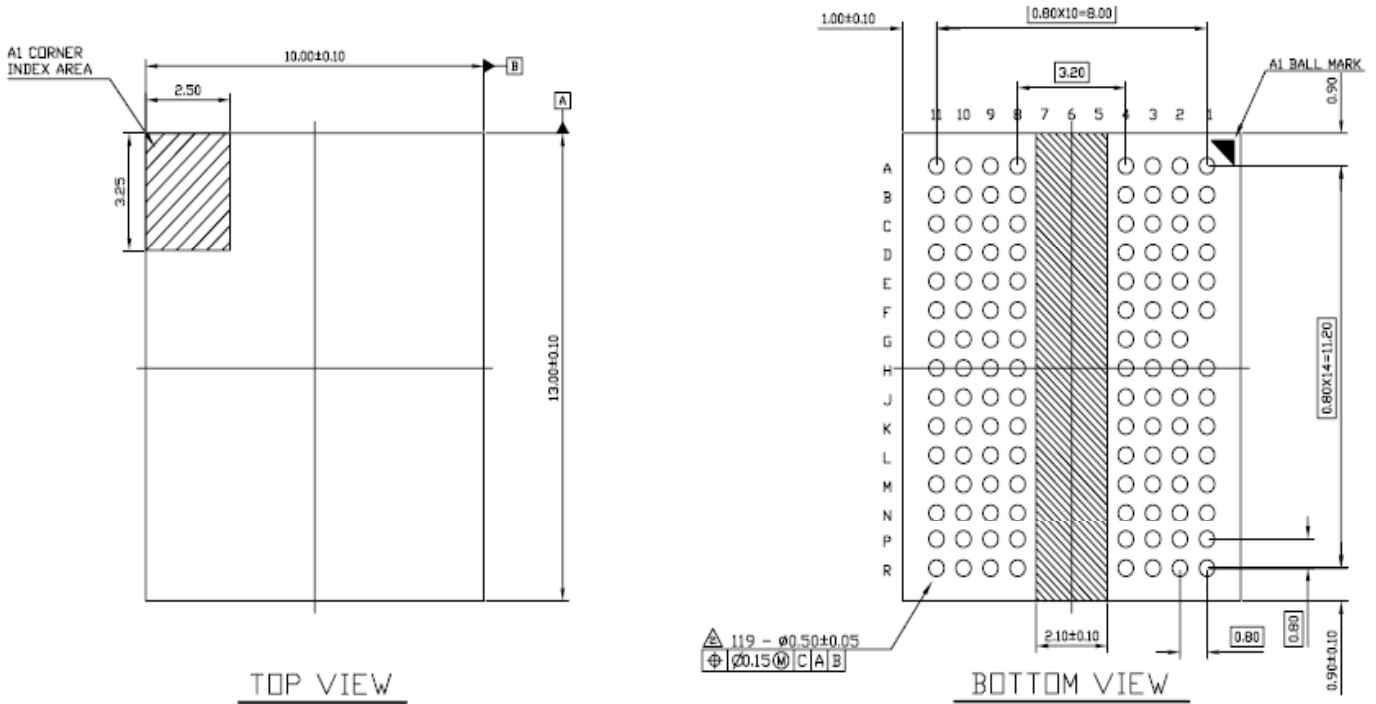
PIN CONFIGURATION(10.0x13.0mm, 119-FBGA)





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Package Drawing(10.0x13.0mm, 119-FBGA)



Description
FBGA 119BALL
Dimension
10.0mm x 13.0mm x 1.45mm(Max)

1. ALL DIMENSIONS are in Millimeters.
2. POST REFLOW SOLDER BALL DIAMETER.
(Pre Reflow diameter : $\text{Ø}0.45\pm0.02$)
3. TOLARENCE INCLUDES WARPAGE.



PIN DESCRIPTION

Pin Name	Function (DDR2 SDRAM)
A0~A13	Address Inputs
BA0, BA1, BA2	Block Select Address
DQ0~DQ15	Data Input/Output
DQS0, DQS0#	Low Data Strobe
DQS1, DQS1#	Up Data Strobe
CS#	Chip Select
RAS#	Row Address Strobe Command
CAS#	Column Address Strobe Command
WE#	Write Enable
DQM1, DQM2	Input Mask
CLK	Clock Input
CLK#	Clock Input
CKE	Clock Enable
VREF	Input Reference Voltage
VDD	Power Supply
VDDQ	Power for DQ Circuit
VSSQ	Ground for DQ Circuit
VDDL	Power for DLL
VSSDL	Ground for DLL
ODT	On-Die Terminal Control

Pin Name	Function (NAND Flash)
IO0~IO7	Input and Output
CE#	Chip Enable
WE#	Write Enable
RE#	Read Enable
ALE	Address Latch Enable
CLE	Command Latch Enable
WP#	Write Protect
R \bar{B}	Ready/Busy
VCC	Power Supply

Pin Name	Function
VSS	Ground
NC	No Connection



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Ordering Information

