Multi-Chip Package MEMORY
2G Bit(256Mx8) NAND Flash / 1G Bit (8Mx16x8Banks) DDR2 SDRAM

Revision No.	History	Draft Date	Remark
Rev 00	Initial Draft	Aug. 2011	Preliminary

Multi-Chip Package MEMORY

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<MCP Features>

• Operating Temperature : 0℃ ~ 85℃
• 119-ball FBGA Type - 10x13mm, 0.8mm pitch

<NAND Features>

- **Power Supply Voltage**
  - 2.7V ~ 3.6V
- **Organization**
  - Memory Cell Array : (2K + 64)Bytes x 64pages x 2048 Blocks
- **Page Size**
  - (2K+64 spare) Bytes
- **Block Size**
  - (128K + 4K spare)Bytes
- **PAGE READ / PROGRAM**
  - Random Access : 25μs (Max.)
  - Sequential Access : 25ns(Min.)
  - Program time : 200μs (Typ.)
  - Multi-page program time(2pages): 200us(Typ.)
- **FAST BLOCK ERASE**
  - Block erase Time : 1.5ms(Typ.)
  - Multi-block erase time (2blocks): 1.5ms(Typ.)
- **COPY BACK PROGRAM MODE**
  - Automatic block download without latency time
- **CACHE READ**
  - Internal(2048+64)Byte buffer to improve the read throughput
- **CHIP ENABLE DON'T CARE**
- **DATA RETENTION**
  - 100K Program/Erase Cycles (with 1bit / 528byte ECC)
  - 10 Years Data Retention

<DDR2 SDR Features>

- **Density:** 1G bits
- **Organization :** 8M × 16 bits × 8 banks
- **Power supply:**1.8V ± 0.1V
- **Data rate:** 667/800 (max.)
- **8 internal memory banks**
- **Programmable CAS Latency:**3,4,5
- **Programmable Additive Latency :** 0,1,2,3,4,5
- **Write Latency =** Read Latency -1
- **Programmable Burst Length :**
  4 and 8 Programmable Sequential / Interleave Burst
- **OCD (Off-chip Driver Impedance Adjustment)**
- **ODT (On-Die Termination)**
- **4n-bit prefetch architecture**
- **Data-Strobes :** Bidirectional, Differential
- **Auto-Refresh and Self-Refresh**
- **Strong and Weak Strength Data-Output Driver**
- **2KB Page Size**
- **7.8us max. Average Periodic Refresh Interval**

MCP Product Information

Part number	NAND Flash		DDR3 SDRAM		Package (FBGA)
	Density	Voltage	Density/Voltage	Speed	
MST7F08F16DMH-266	2G bit(x8)	2.7 – 3.6V	1Gbit(x16) / 1.8V	667Mbps	10x13mm 119 ball
MST7F08F16DMH-280	2G bit(x8)	2.7 – 3.6V	1Gbit(x16) / 1.8V	800Mbps	10x13mm 119 ball

PIN CONFIGURATION(10.0x13.0mm, 119-FBGA)

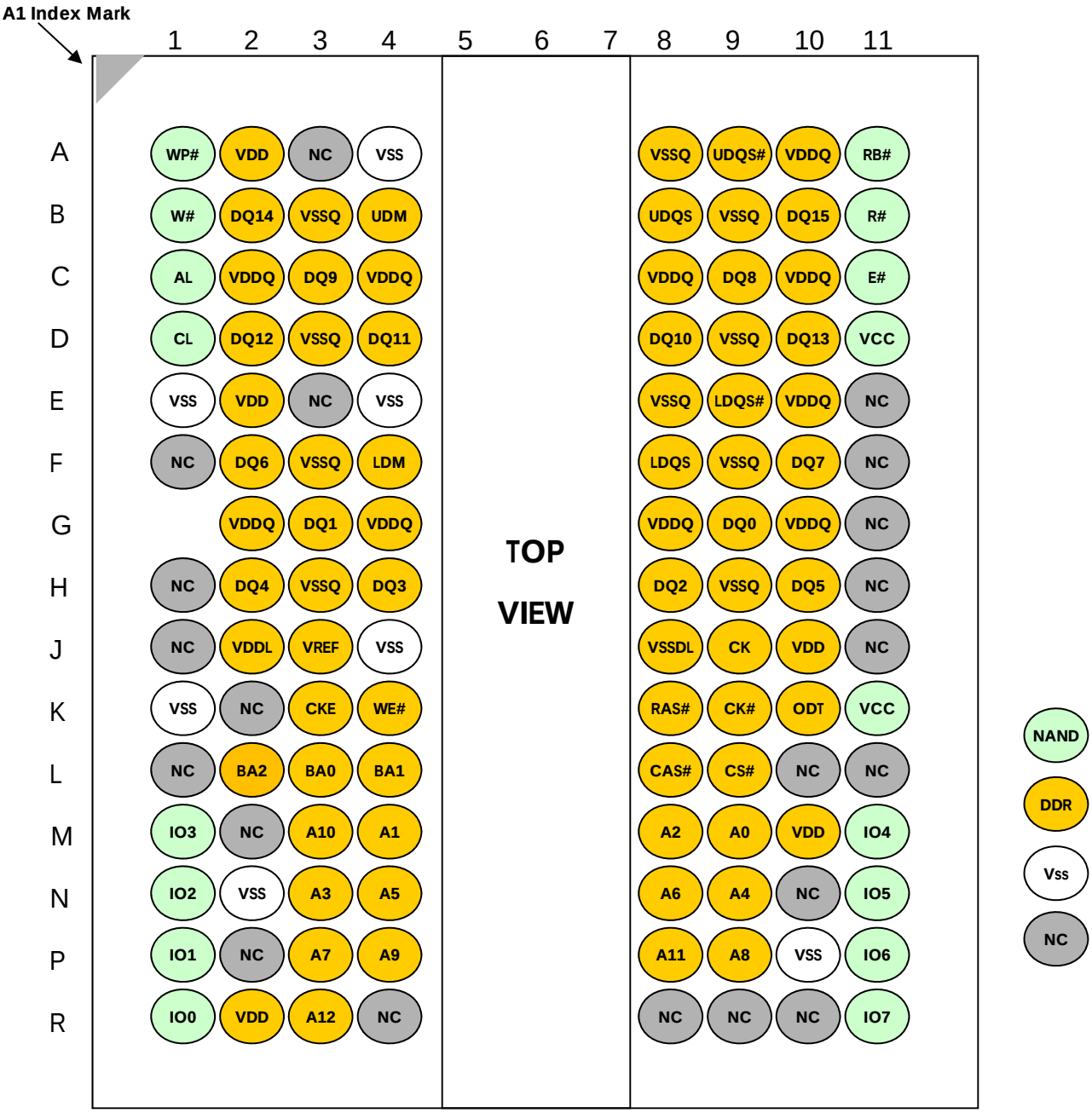
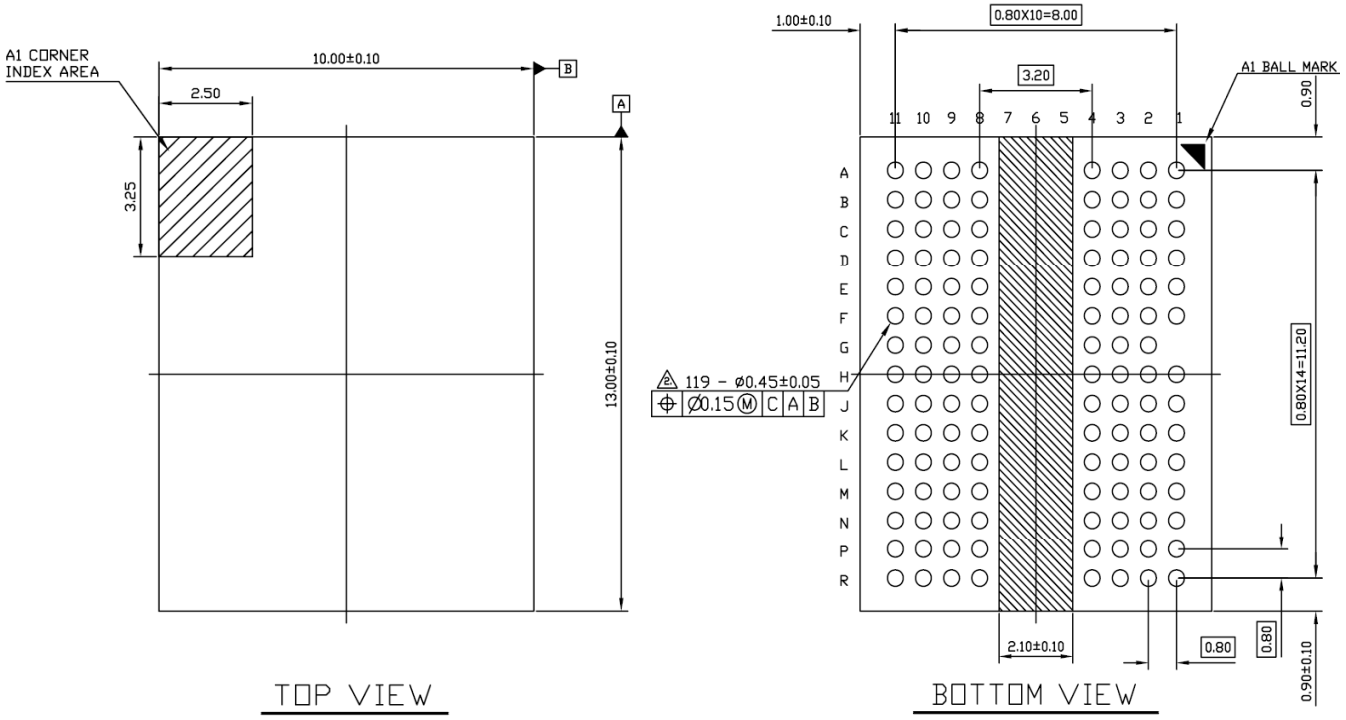
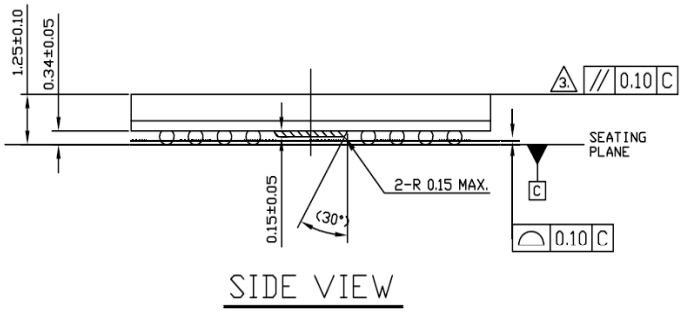


Figure1: Pin Configuration

Package Outline Drawing(10.0x13.0mm, 119-FBGA)





Description
FBGA 119BALL
Dimension
10.0mm x 13.0mm x 1.35mm (max)

1. **ALL DIMENSIONS are in Millimeters.**
2. **POST REFLOW SOLDER BALL DIAMETER.**
   (Pre Reflow diameter : Ø0.45±0.02)
3. **TOLARENCE INCLUDES WARPAGE.**

Figure2: Package Outline Drawing

PIN DESCRIPTION

Pin Name	Function (DDR2 SDRAM)
A0~A12	Address Inputs
BA0, BA1, BA2	Block Select Address
DQ0~DQ15	Data Input/Output
LDQS, $\overline{\text{LDQS}}$	Low Data Strobe
UDQS, $\overline{\text{UDQS}}$	Up Data Strobe
$\overline{\text{CS}}$	Chip Select
$\overline{\text{RAS}}$	Row Address Strobe Command
$\overline{\text{CAS}}$	Column Address Strobe Command
$\overline{\text{WE}}$	Write Enable
LDM, UDM	Input Mask
CLK	Clock Input
CLK#	Clock Input
CKE	Clock Enable
VREF	Input Reference Voltage
VDD	Power Supply
VDDQ	Power for DQ Circuit
VSSQ	Ground for DQ Circuit
VDDL	Power for DLL
VSSDL	Ground for DLL
ODT	On-Die Terminal Control

Pin Name	Function (NAND Flash)
IO0~IO7	Input and Output
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{WE}}$	Write Enable
$\overline{\text{RE}}$	Read Enable
ALE	Address Latch Enable
CLE	Command Latch Enable
$\overline{\text{WP}}$	Write Protect
R/$\overline{\text{B}}$	Ready/Busy
VCC	Power Supply

Pin Name	Function
VSS	Ground
NC	No Connection

Ordering Information

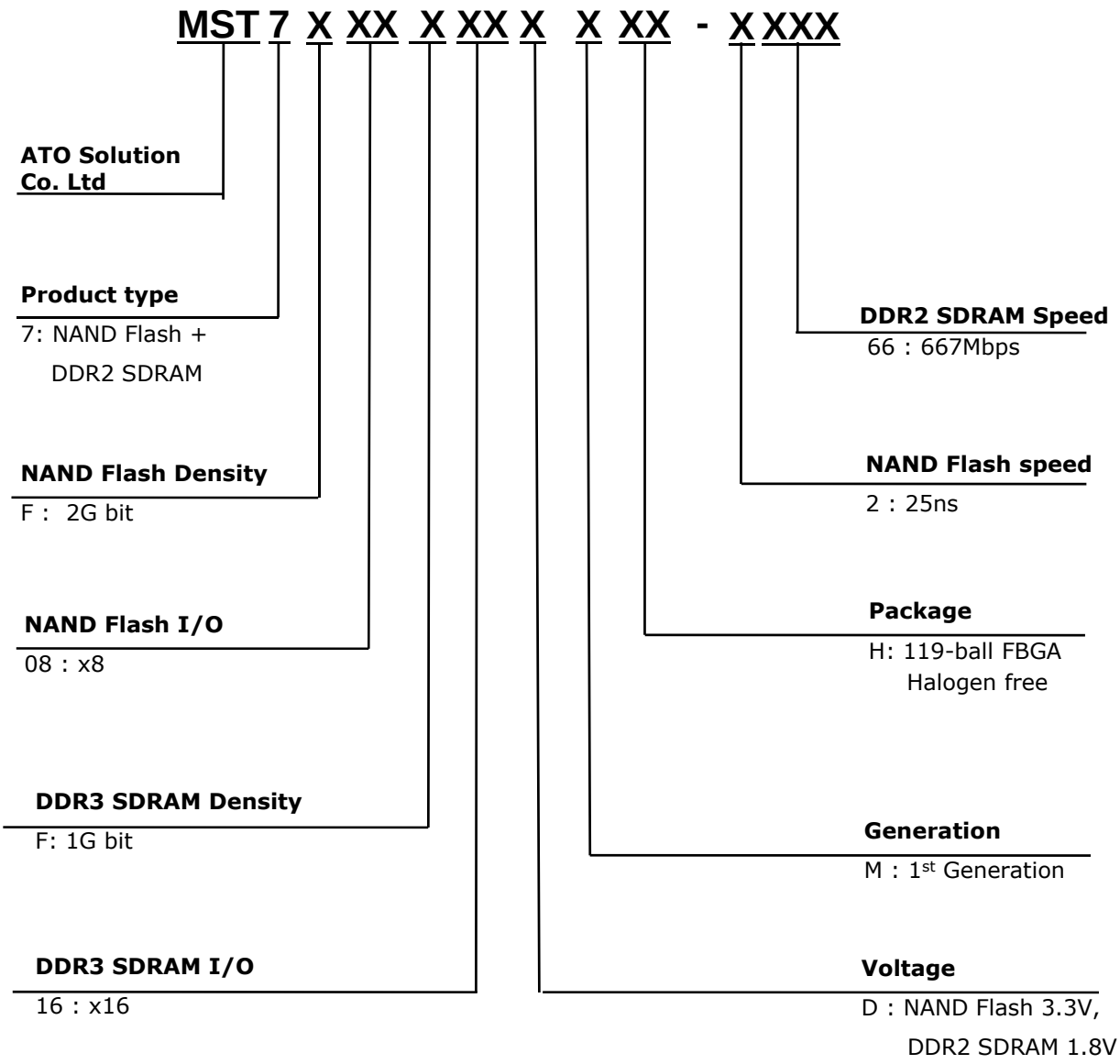


Figure3: Ordering Information