Multi-Chip Package MEMORY
512M Bit(64Mx8) NAND Flash / 2G Bit (16Mx16x8Banks) DDR3 SDRAM

Revision No.	History	Draft Date	Remark
Rev 00	Initial Draft	Jul. 2012	Preliminary
Rev 01	Adjust DRAM parameter of 42nm product	Sep. 2012	

Multi-Chip Package MEMORY

512M Bit (64Mx8) NAND Flash / 2G Bit (16Mx16x8Banks) DDR3 SDRAM

<MCP Features>

• Operating Temperature : 0℃ ~ 85℃
• 119-ball FBGA Type - 10x13mm, 0.8mm pitch

<NAND Features>

- **Power Supply Voltage**
  - 2.7V ~ 3.6V
- **Organization**
  - Memory Cell Array : (64M + 2M)bit x 8 bit
- **Data Register : (512 + 16)bit x 8 bit**
- **Automatic Program and Erase**
  - Page Program : (512 + 16)Byte
  - Block Erase : (16K + 512)Byte
- **Page Read Operation**
  - Page Size : (512 + 16)Byte
  - Random Access : 15μs (Max.)
  - Serial Page Access : 30ns(Min.)
- **Fast Write Cycle Time**
  - Program time : 200μs (Typ.)
  - Block Erase Time : 2ms(Typ.)
- **Copy-Back Program Operation**
- **Hardware Data Protection**
  - Program/Erase Lockout During Power Transitions
- **Data Integrity**
  - Endurance : 100K Program/Erase Cycles
  - Data Retention : 10 Years
- **Command Register Operation**

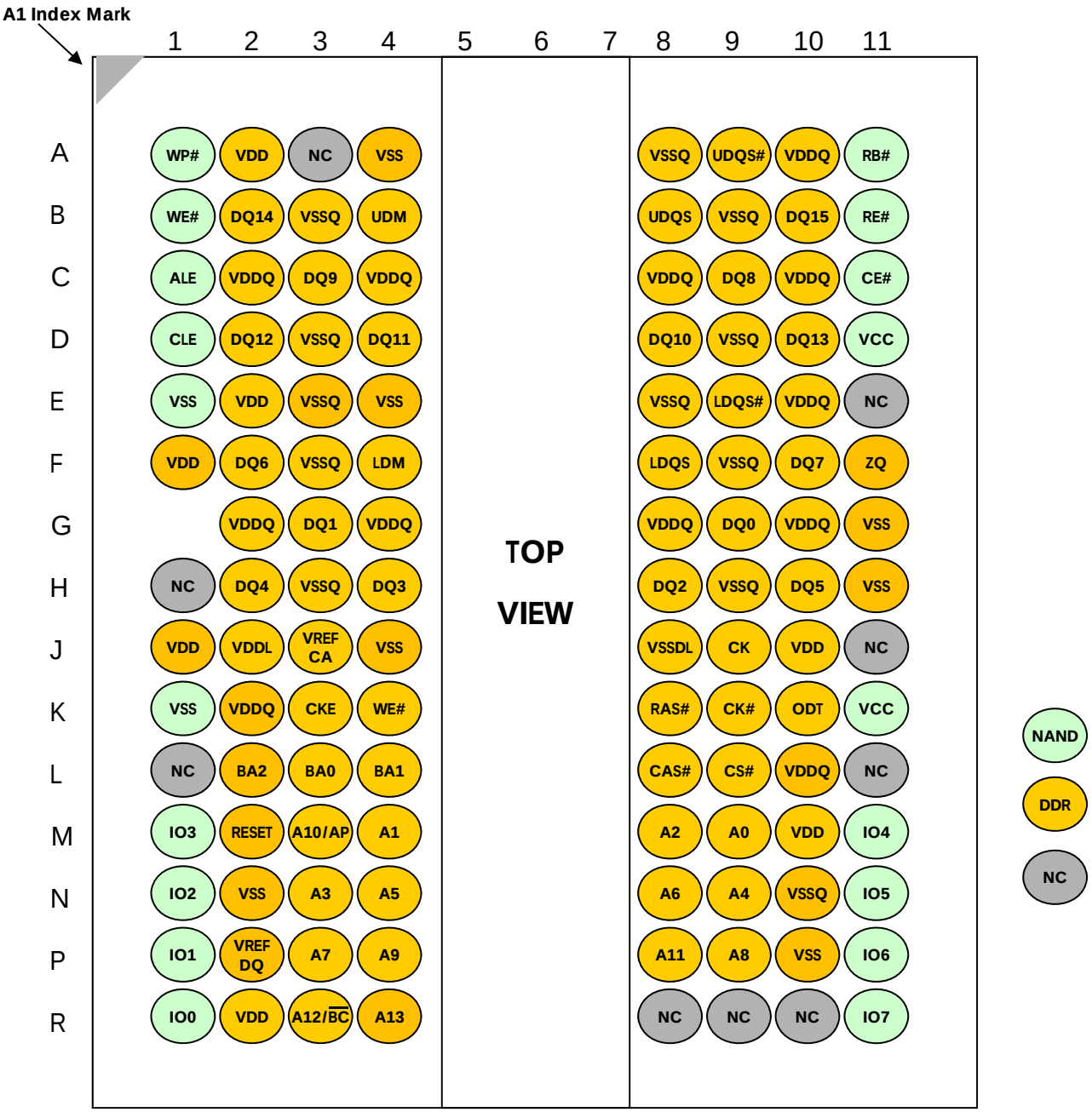
•<DDR3 SDR Features>

- **Density: 2G bits**
- **Organization : 16M × 16 bits × 8 banks**
- **Power supply:1.5V ± 0.075V**
- **Data rate: 1066 (max.)**
- **8 internal memory banks**
- **Programmable CAS Latency:5,6,7,8,9,10,11,12**
- **CAS WRITE Latency(CWL) : 5,6,7,8,9**
- **POSTED CAS ADDITIVE Programmable Additive Latency : 0, CL-1, CL-2 clock**
- **Programmable Sequential/Interleave Burst Type**
- **Programmable Burst Length : 4,8**
- **Output Driver Impedance Control**
- **Differential bidirectional data strobe through ZQ Pin (RZQ : 240 ohm±1%)**
- **OCD calibration**
- **Dynamic ODT (Rtt_Nom & Rtt_WR)**
- **Auto Self-Refresh**
- **Self-Refresh Temperature**

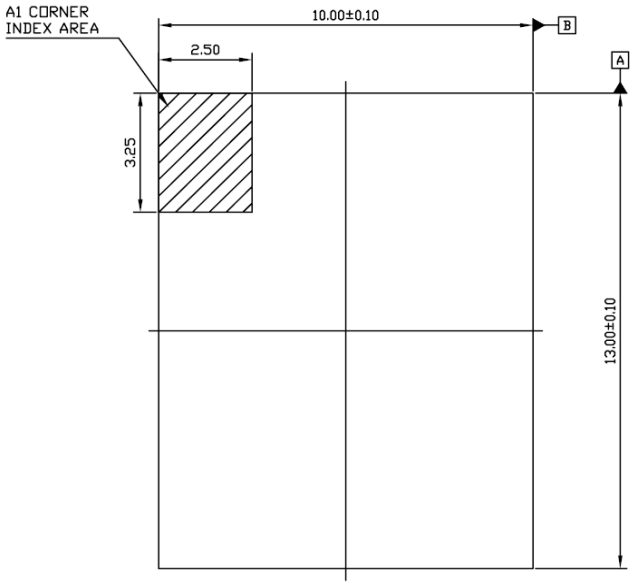
MCP Product Information

Part number	NAND Flash		DDR3 SDRAM		Package (FBGA)
	Density	Voltage	Density/Voltage	Speed	
MST5B08G16GMH-3106	512M bit(x8)	2.7 – 3.6V	2Gbit(x16) / 1.5V	1066Mbps	10x13mm 119 ball

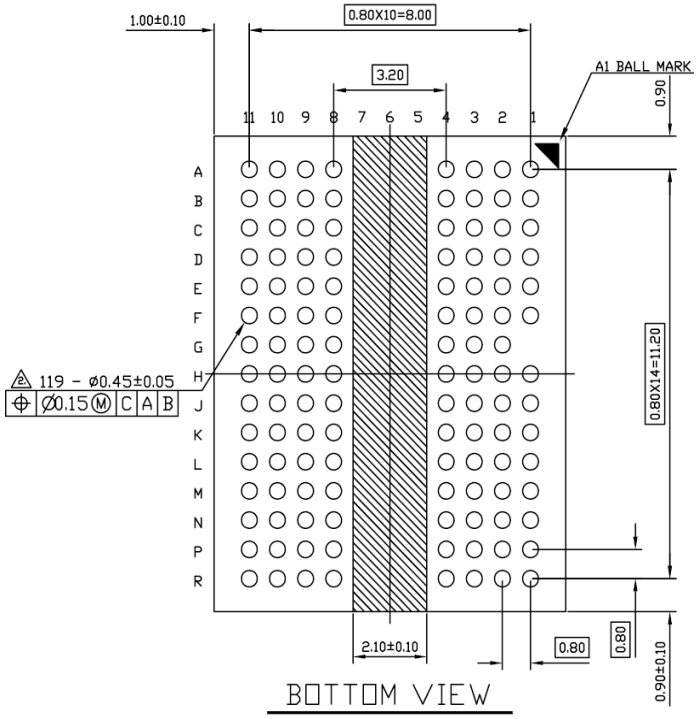
PIN CONFIGURATION(10.0x13.0mm, 119-FBGA)



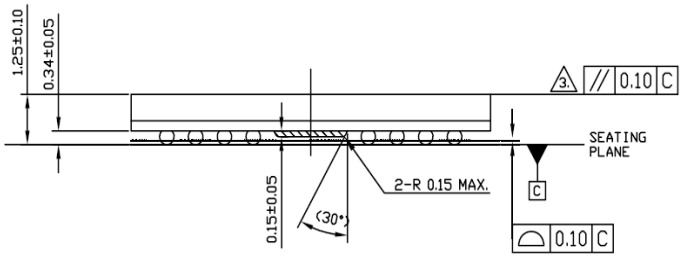
Package Drawing(10.0x13.0mm, 119-FBGA)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Description
FBGA 119BALL
Dimension
10.0mm x 13.0mm x 1.35mm (max)

1. **ALL DIMENSIONS are in Millimeters.**
2. **POST REFLOW SOLDER BALL DIAMETER.**
   (Pre Reflow diameter : Ø0.45±0.02)
3. **TOLARENCE INCLUDES WARPAGE.**

PIN DESCRIPTION

<DDR3 SDRAM>

Pin Name	Description
CK, CK#	Clock
CKE	Clock Enable
CS	Chip Select
RAS, CAS, WE	Command Input
UDM, LDM	Input Data Mask
BA0 – BA2	Bank Address Input
A10/AP	Auto-Precharge
A0 – A13	Address Inputs
$\overline{A12}$/BC	Burst Chop
ODT	On Die Termination
RESET	Active Low Asynchronous Reset
DQ0 – DQ15	Data Inputs/Outputs
LDQS/UDQS LDQS#/UDQS#	Data Strobe
VDDQ	DQ Power Supply
VDD	Power Supply
VSSQ	DQ Ground
VSS	Ground
VREFCA	Reference voltage for CA
VREFDQ	Reference voltage for DQ
VDDL	Power for DLL
VSSDL	Ground for DLL
ZQ	Reference pin for ZQ calibration

<NAND FLASH>

Pin Name	Description
IO0 – IO7	Input and Output
CE#	Chip Enable
WE#	Write Enable
RE#	Read Enable
ALE	Address Latch Enable
CLE	Command Latch Enable
WP#	Write Protect
R/B#	Ready/Busy
VCC	Power Supply

Pin Name	Description
NC	No Connection

Ordering Information