



2Gb NAND FLASH + 1Gb DDR3 SDRAM MCP Product

Multi-Chip Package MEMORY

2G Bit(256Mx8) NAND Flash / 1G Bit (8Mx16x8Banks) DDR3 SDRAM

Revision No.	History	Draft Date	Remark
Rev 00	Initial Draft	June. 2012	Preliminary



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<MCP Features>

- Operating Temperature : 0°C ~ 85°C
- 119-ball FBGA Type - 10x13mm, 0.8mm pitch

<NAND Features>

- . **Power Supply Voltage**
 - 2.7V ~ 3.6V
- . **Organization**
 - Memory Cell Array : (128M + 4M)bit x 8 bit
- . **Data Register : (2048 + 64)bit x 8 bit**
- . **Automatic Program and Erase**
 - Page Program : (2048 + 64)Byte
 - Block Erase : (128K + 4K)Byte
- . **Page Read Operation**
 - Page Size : (2048 + 64)Byte
 - Random Access : 25μs (Max.)
 - Serial Page Access : 25ns (Min.)
- . **Fast Write Cycle Time**
 - Program time : 200μs (Typ.)
 - Block Erase Time : 2ms (Typ.)
- . **Command/Address/Data Multiplexed I/O Port**
- . **Hardware Data Protection**
 - Program/Erase Lockout During Power Transitions
- . **Data Integrity**
 - Endurance : 100K Program/Erase Cycles (with 1 bit / 528byte ECC)
 - Data Retention : 10 Years
- . **Command Register Operation**

•<DDR3 SDR Features>

- **Density: 1G bits**
- **Organization : 8M × 16 bits × 8 banks**
- **Power supply: 1.5V ± 0.075V**
- **Data rate: 1066 (max.)**
- **8 internal memory banks**
- **Programmable CAS Latency: 5, 6, 7, 8, 9, 10, 11, 12, 13**
- **POSTED CAS ADDITIVE Programmable Additive Latency : 0, CL-1, CL-2**
- **Programmable Sequential/Interleave Burst Type**
- **Programmable Burst Length : 4, 8**
- **Output Driver Impedance Control**
- **Differential bidirectional data strobe**
- **OCD calibration**
- **Dynamic ODT (Rtt_Nom & Rtt_WR)**
- **Auto Self-Refresh**
- **Self-Refresh Temperature**



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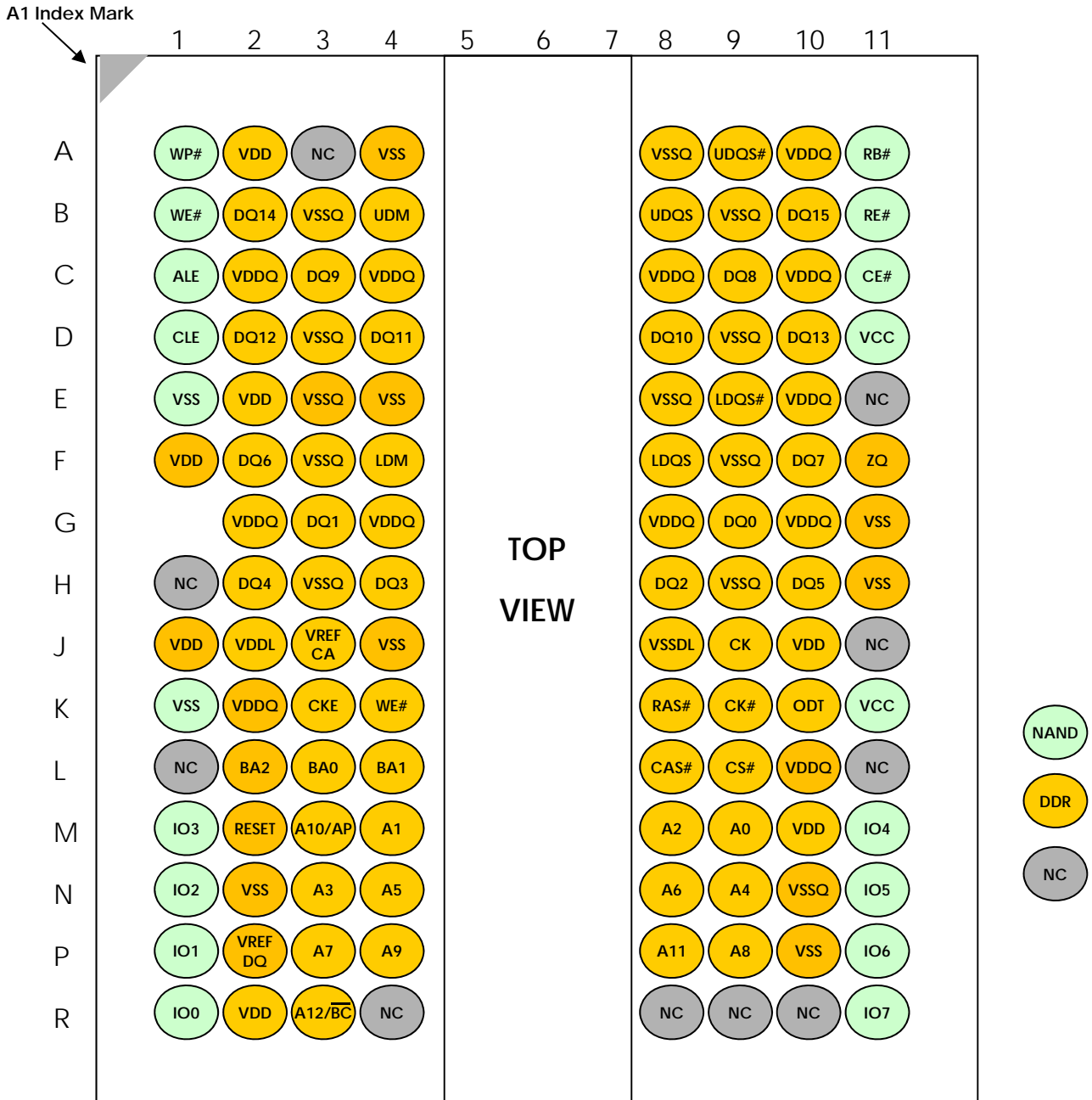
MCP Product Information

Part number	NAND Flash		DDR3 SDRAM		Package (FBGA)
	Density	Voltage	Density/Voltage	Speed	
MST5F08F16GMH-2106	2G bit(x8)	2.7 - 3.6V	1Gbit(x16) / 1.5V	1066Mbps	10x13mm 119 ball



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PIN CONFIGURATION(10.0x13.0mm, 119-FBGA)





PIN DESCRIPTION

<DDR3 SDRAM>

Pin Name	Description
CK, CK#	Clock
CKE	Clock Enable
CS	Chip Select
RAS, CAS, WE	Command Input
UDM, LDM	Input Data Mask
BA0 – BA2	Bank Address Input
A10/AP	Auto-Precharge
A0 – A12	Address Inputs
$\overline{A12}$ /BC	Burst Chop
ODT	On Die Termination
RESET	Active Low Asynchronous Reset
DQ0 – DQ15	Data Inputs/Outputs
LDQS/UDQS LDQS#/UDQS#	Data Strobe
VDDQ	DQ Power Supply
VDD	Power Supply
VSSQ	DQ Ground
VSS	Ground
VDDL	Power for DLL
VSSDL	Ground for DLL
VREFCA	Reference voltage for CA
VREFDQ	Reference voltage for DQ
ZQ	Reference pin for ZQ calibration

<NAND FLASH>

Pin Name	Description
I00 – I07	Input and Output
CE#	Chip Enable
WE#	Write Enable
RE#	Read Enable
ALE	Address Latch Enable
CLE	Command Latch Enable
WP#	Write Protect
R/B#	Ready/Busy
VCC	Power Supply

Pin Name	Description
NC	No Connection



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Ordering Information

