Multi-Chip Package MEMORY
2G Bit(256Mx8) NAND Flash / 2G Bit (16Mx16x8Banks) DDR3 SDRAM

Revision No.	History	Draft Date	Remark
Rev 00	Initial Draft	Sep. 2012	Preliminary

Multi-Chip Package MEMORY

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<MCP Features>

- Operating Temperature : 0℃ ~ 85℃
- 119-ball FBGA Type - 10x13mm, 0.8mm pitch

<NAND Features>

- **Power Supply Voltage**
  - 2.7V ~ 3.6V
- **Organization**
  - Memory Cell Array : (2K + 64)Bytes x 64pages x 2048 Blocks
- **Page Size**
  - (2K+64 spare) Bytes
- **Block Size**
  - (128K + 4K spare)Bytes
- **PAGE READ / PROGRAM**
  - Random Access : 25μs (Max.)
  - Sequential Access : 25ns(Min.)
  - Program time : 200μs (Typ.)
  - Multi-page program time(2pages): 200us(Typ.)
- **FAST BLOCK ERASE**
  - Block erase Time : 1.5ms(Typ.)
  - Multi-block erase time (2blocks): 1.5ms(Typ.)
- **COPY BACK PROGRAM MODE**
  - Automatic block download without latency time
- **CACHE READ**
  - Internal(2048+64)Byte buffer to improve the read throughput
- **CHIP ENABLE DON'T CARE**
- **DATA RETENTION**
  - 100K Program/Erase Cycles (with 1bit / 528byte ECC)
  - 10 Years Data Retention

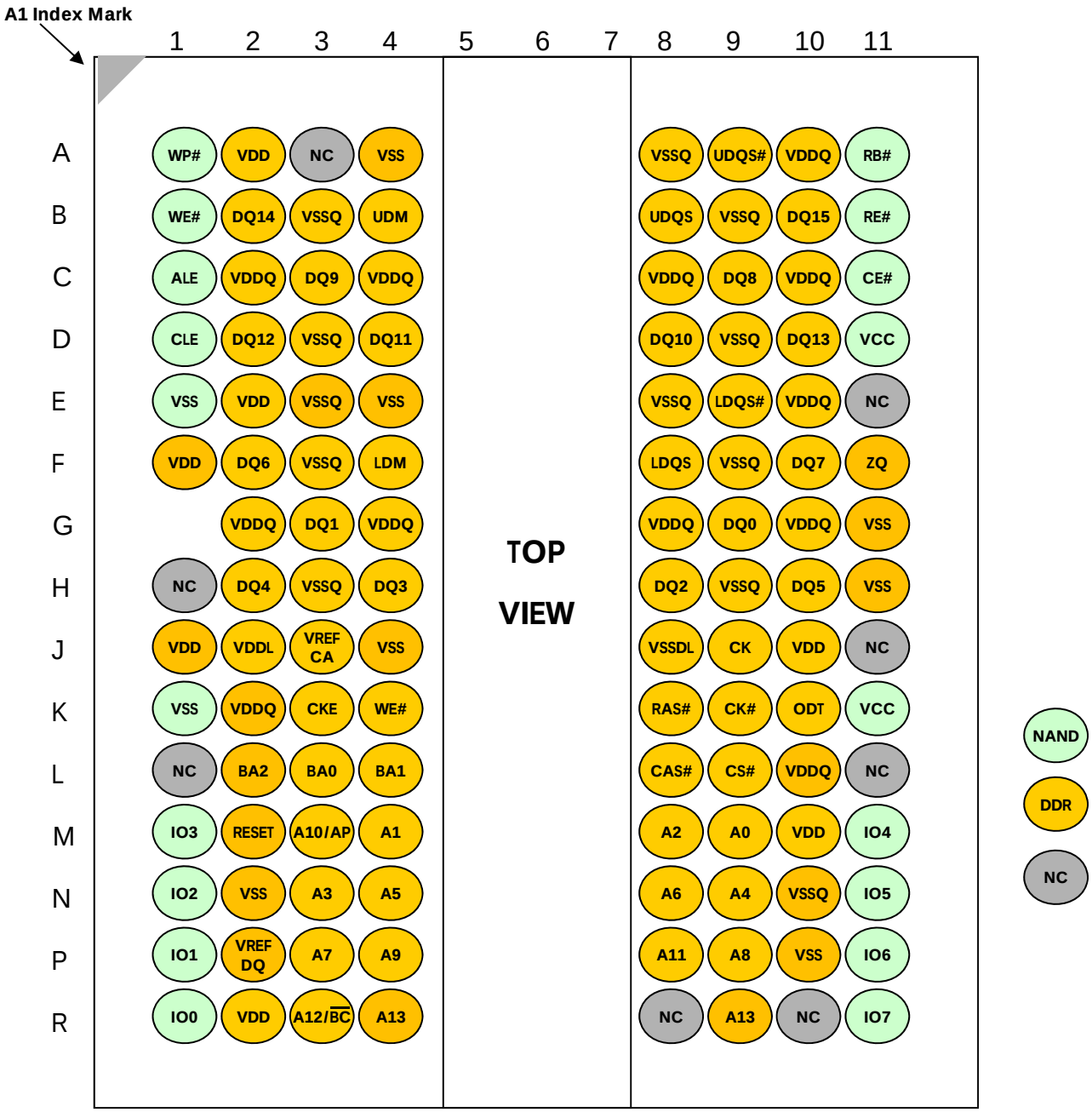
<DDR3 SDR Features>

- **Density: 2G bits**
- **Organization : 16M × 16 bits × 8 banks**
- **Power supply:1.5V ± 0.075V**
- **Data rate: 1066 (max.)**
- **Fully differential clock inputs (CK, $\overline{CK}$) operation**
- **Differential Data Strobe (DQS, $\overline{DQS}$)**
- **On chip DLL align DQ, DQS and $\overline{DQS}$ transition with CK transition**
- **Programmable $\overline{CAS}$ Latency:5,6,7,8,9,10,11,12 13 and 14 supported**
- **DM masks write data-in at the both rising and falling edges of the data strobe**
- **All address and control inputs except data, data strobes and data masks latched on the rising edges of the clock**
- **Programmable CAS WRITE Latency(CWL) : 5,6,7,8,9,10**
- **Programmable Additive Latency : 0, CL-1, CL-2 supported**
- **Programmable burst length 4/8 with both nibble sequential and interleave mode**
- **BL switch on the fly**
- **Auto Self Refresh supported**
- **Driver strength selected by EMRS**
- **Dynamic On Die Termination(ODT) supported**
- **ZQ calibration supported**
- **8bit pre-fetch**

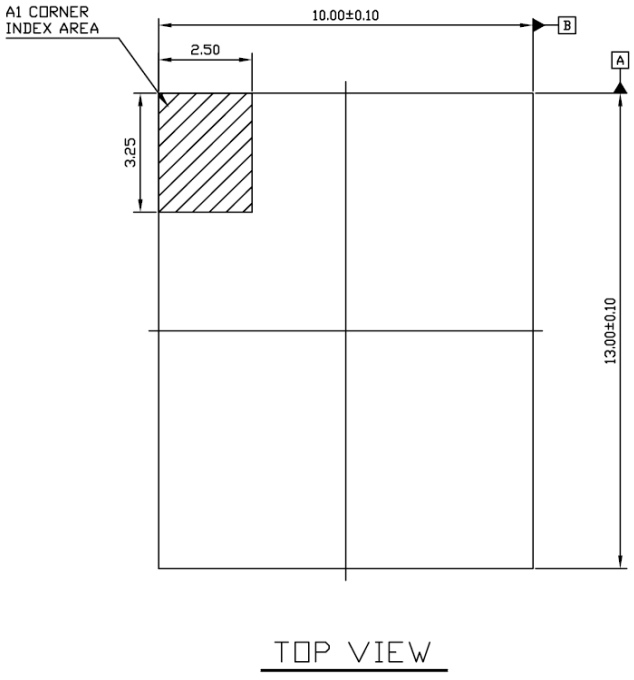
MCP Product Information

Part number	NAND Flash		DDR3 SDRAM		Package (FBGA)
	Density	Voltage	Density / Voltage	Speed	
MST5F08G16GNH-2106	2G bit(x8)	2.7 – 3.6V	2Gbit(x16) / 1.5V	1066Mbps	10x13mm 119 ball

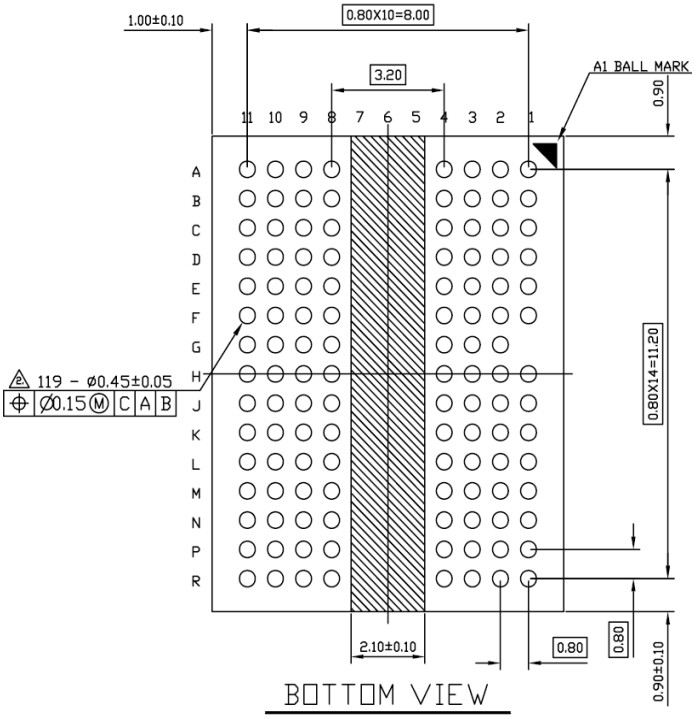
PIN CONFIGURATION(10.0x13.0mm, 119-FBGA)



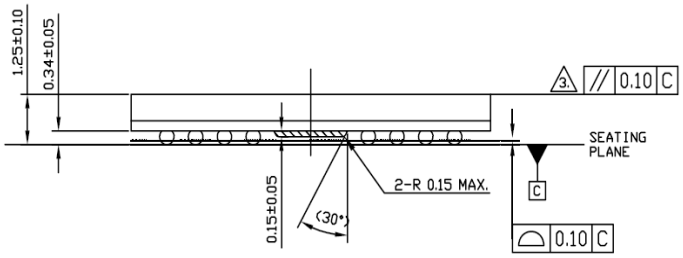
Package Drawing(10.0x13.0mm, 119-FBGA)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Description
FBGA 119BALL
Dimension
10.0mm x 13.0mm x 1.35mm (max)

1. **ALL DIMENSIONS are in Millimeters.**
2. **POST REFLOW SOLDER BALL DIAMETER.**
   (Pre Reflow diameter : Ø0.45±0.02)
3. **TOLARENCE INCLUDES WARPAGE.**

PIN DESCRIPTION

<DDR3 SDRAM>

Pin Name	Description
CK, CK#	Clock
CKE	Clock Enable
CS	Chip Select
RAS#, CAS#, WE#	Command Input
UDM, LDM	Input Data Mask
BA0 – BA2	Bank Address Input
A10/AP	Auto-Precharge
A0 – A13	Address Inputs
A12/$\overline{BC}$	Burst Chop
ODT	On Die Termination
RESET	Active Low Asynchronous Reset
DQ0 – DQ15	Data Inputs/Outputs
LDQS/UDQS LDQS#/UDQS#	Data Strobe
VDDQ	DQ Power Supply
VDD	Power Supply
VSSQ	DQ Ground
VSS	Ground
VREFCA	Reference voltage for CA
VREFDQ	Reference voltage for DQ
VDDL	Power for DLL
VSSDL	Ground for DLL
ZQ	Reference pin for ZQ calibration

<NAND FLASH>

Pin Name	Description
IO0 – IO7	Input and Output
CE#	Chip Enable
WE#	Write Enable
RE#	Read Enable
ALE	Address Latch Enable
CLE	Command Latch Enable
WP#	Write Protect
R/B#	Ready/Busy
VCC	Power Supply

Pin Name	Description
NC	No Connection

Ordering Information