1Gb NAND FLASH

AFND1G08U3

Revision No.	History	Draft Date	Remark
Rev.00	Initial Draft	June. 2012	Preliminary
Rev.01	Add new FBGA PKG dimension option (6.5x8.0mm 48B)	Nov. 2012	

FEATURES SUMMARY

- **Power Supply**

-3.3V Device(AFND1G08U3) 2.7V ~ 3.6V

- **Organization**

-Memory Cell Array : (128M + 4M) x 8bits
-Data Register : (2048 + 64) x 8bits

- **Automatic Program and Erase**

-Page Program : (2048 + 64) x 8bits
-Block Erase : (128K +4K) x 8bit = 64pages

- **Page Read Operation**

-Page Size : (2048 + 64) x 8bits
-Random Access : 25us(Max.)
-Serial Page Access : 25ns(Min.)

- **Fast Write Cycle Time**

-Program time : 200us(Typ.)
-Block Erase time : 2ms(Typ.)

- **Copy-Back PROGRAM Operation**

- Fast Page copy without external buffering

- **Status Register**

- Normal Status Register (Read/Program/Erase)

- **Security features**

-OTP area, 16Kbytes(8 pages)

- **Hardware Data Protection**

-Program / Erase locked during Power transitions

- **Data Integrity**

-Endurance : 100K Program / Erase Cycles
(With 1bit/528byte ECC)
-Data Retention : 10 years

- **Package**

-AFND1G08U3 : Pb-Free Package
48-pin TSOP(12 x 20 / 0.5 mm pitch)
48-Ball FBGA: 9.0 x 9.0 x 1.0mm
48-Ball FBGA: 6.5 x 8.0 x 1.0mm

Product Information

Part number	Voltage	Bus Width	Package
AFND1G08U3-CKA	2.7~3.6V	x8	12x20mm TSOP
AFND1G08U3-CKC			9.0x9.0mm FBGA
AFND1G08U3-CKD			6.5x8.0mm FBGA

GENERAL DESCRIPTION

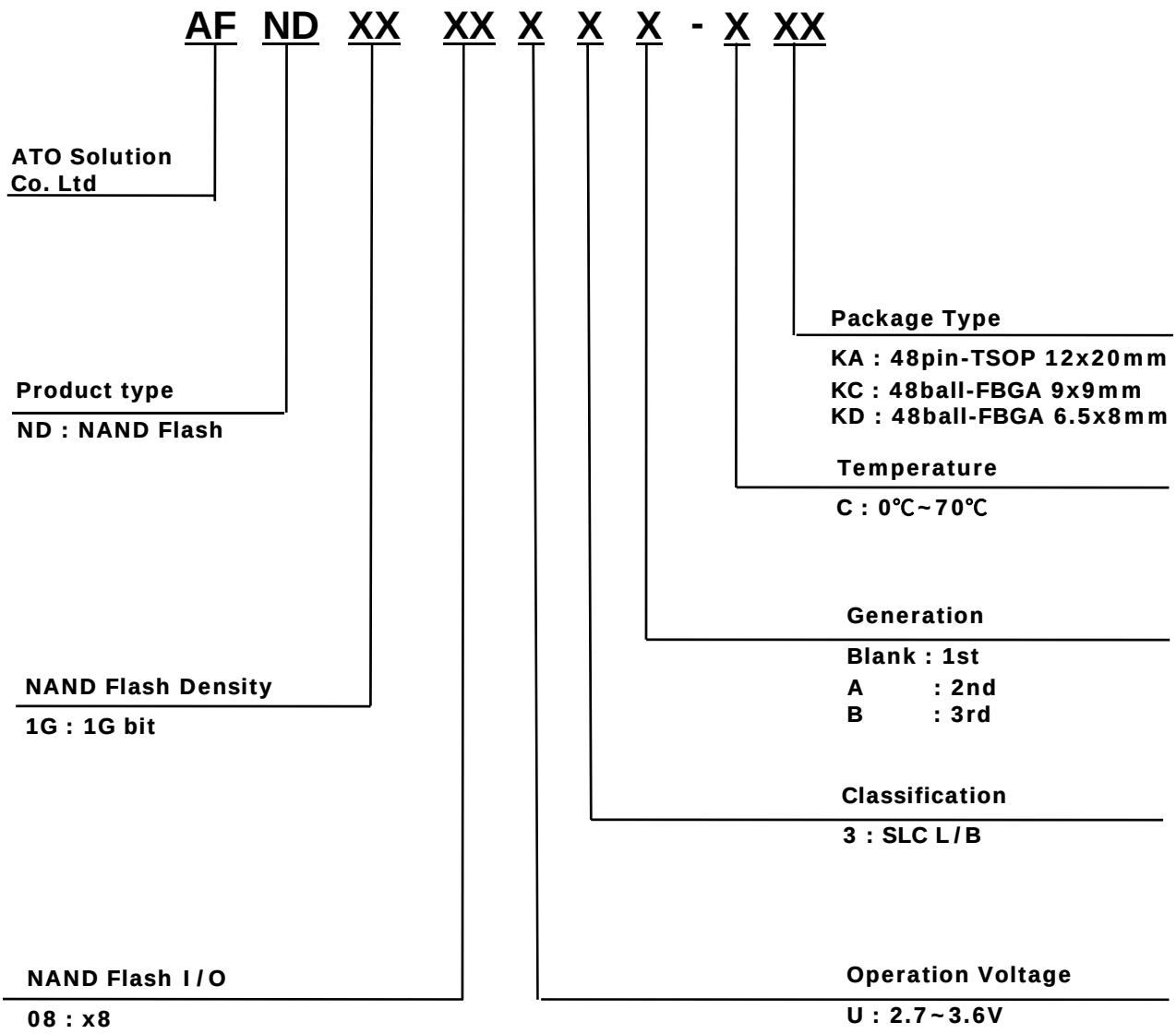
The AFND1G08U3 is 1G-bit with spare 32Mbit capacity. The device is offered in 3.3V power supply. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it possible to preserve valid data while old data is erased. The device contains 1024 blocks, composed by 64 pages consisting in two NAND structures of 16 series connected Flash Cells. A program operation can be performed in typical 200us on the 2048-bytes and an erase operation can be performed in typical 2ms on a 128K-bytes block. Data in the page can be read out at 25ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. Command, Data and Address are synchronously introduced using /CE, /WE, ALE and CLE input pin. The output pin R/B(open drain buffer) signals the status of the device during each operation. In a system with multiple memories the R/B pins can be connected all together to provide a global status signal. The on-chip write control automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the AFND1G08U3's extended reliability of 100K program / erase cycles by providing ECC(Error Correction Code) with real time mapping-out algorithm.

The chip could be offered with the /CE don't care function. This function allows the direct download of the code form the NAND flash memory device by a microcontroller, since the /CE transitions do not stop the read operation.

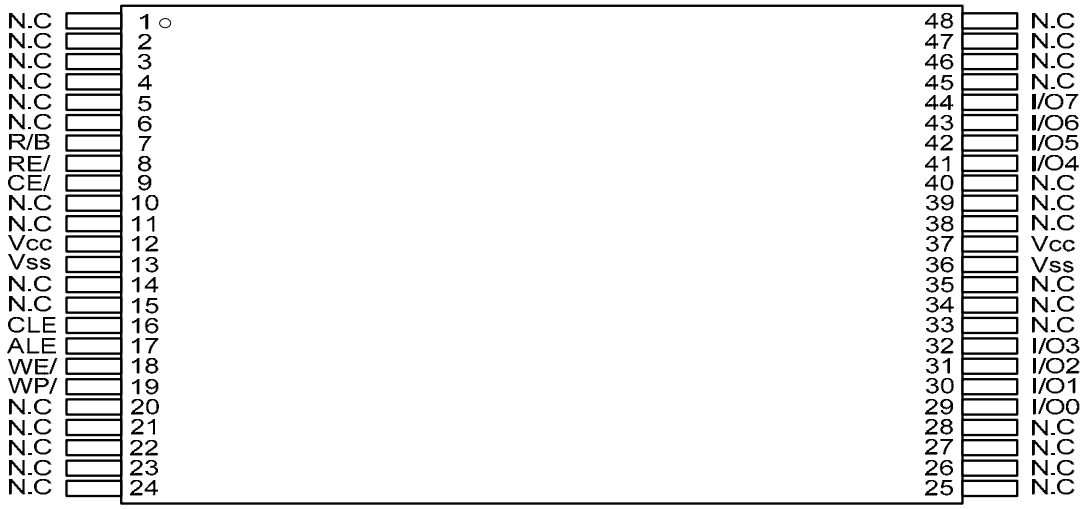
The copy back function allows the optimization of defective blocks management : when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. Also, this device includes extra features like OTP area, Block mechanism.

The AFND1G08U3 is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

Ordering Information

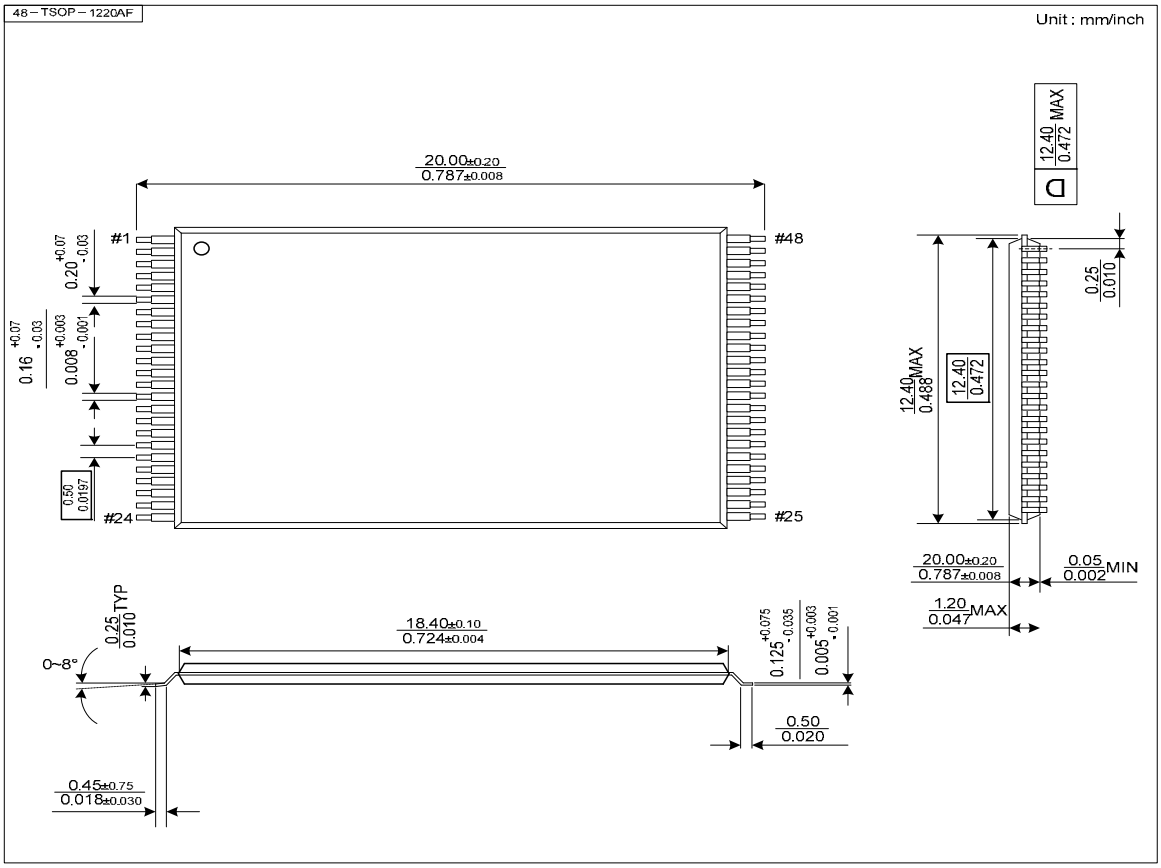


PIN CONFIGURATION (TSOP1)

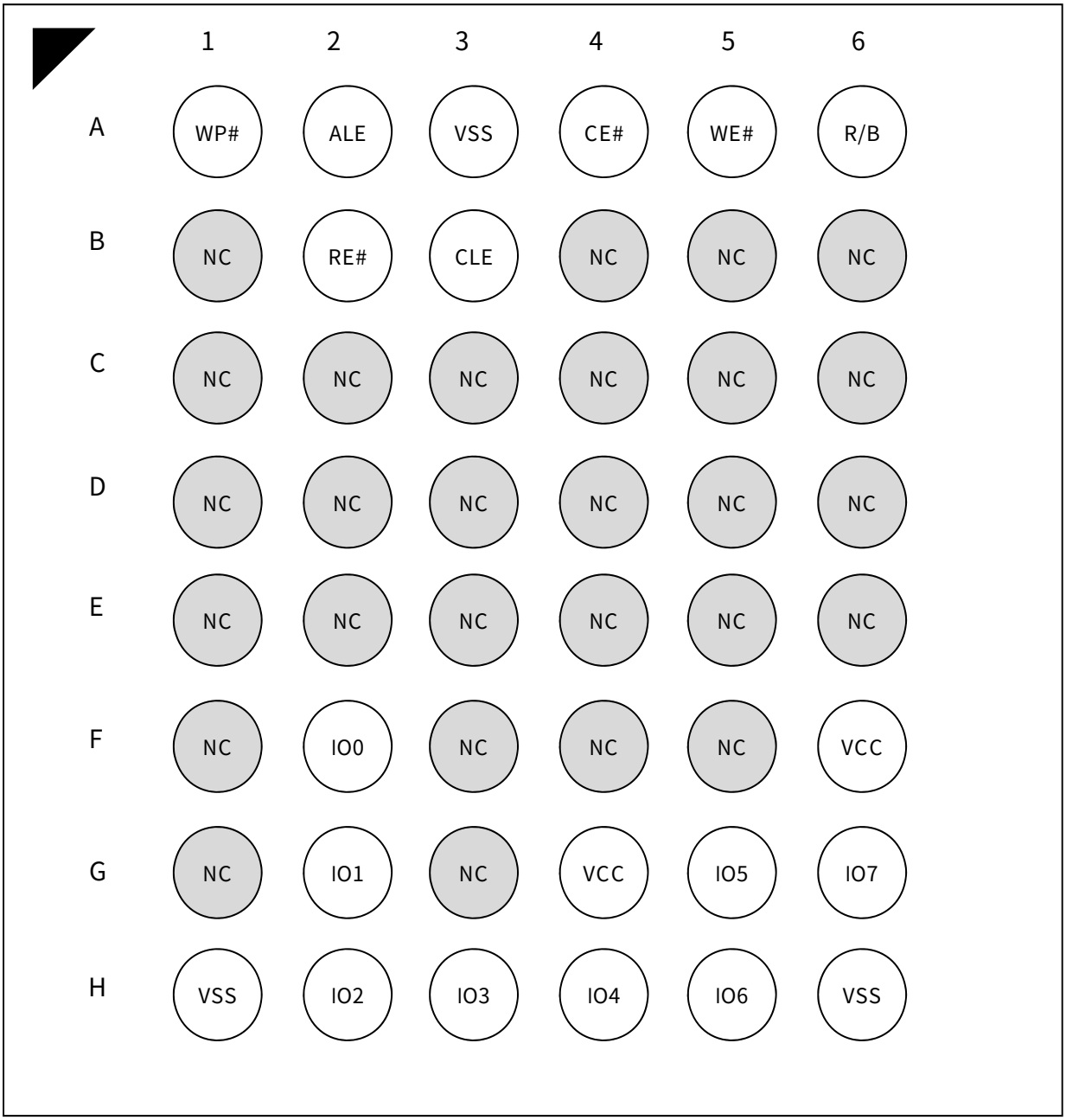


PACKAGE DIMENSIONS

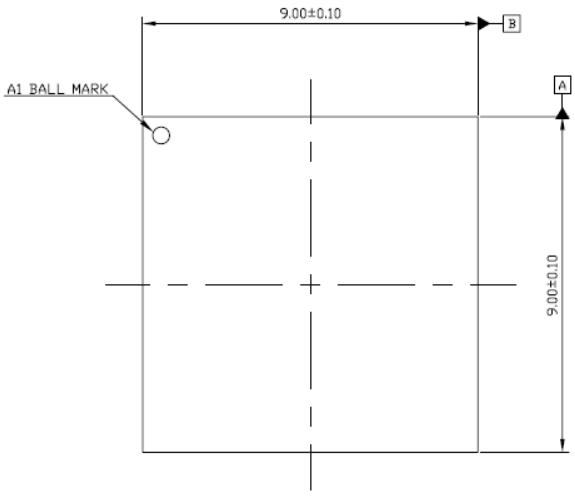
48-PIN LEAD/LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)



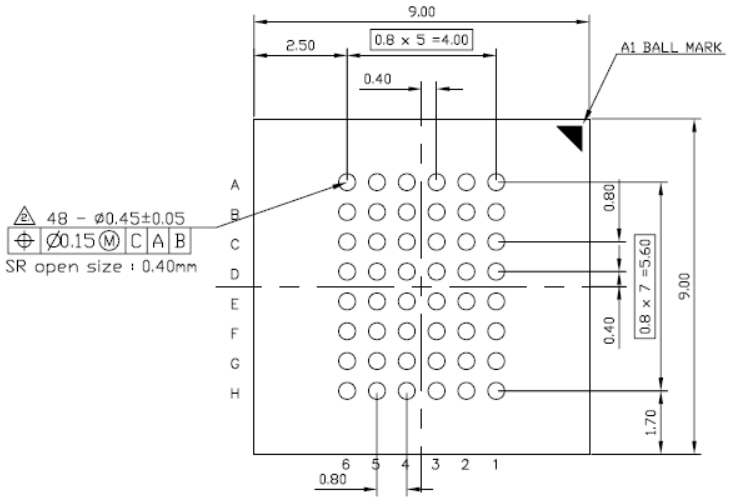
PIN CONFIGURATION (48ball-FBGA)



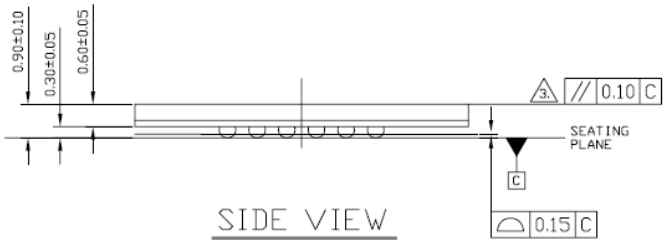
PACKAGE OUTLINE DRAWING (48ball-FBGA 9x9mm)



TOP VIEW



BOTTOM VIEW

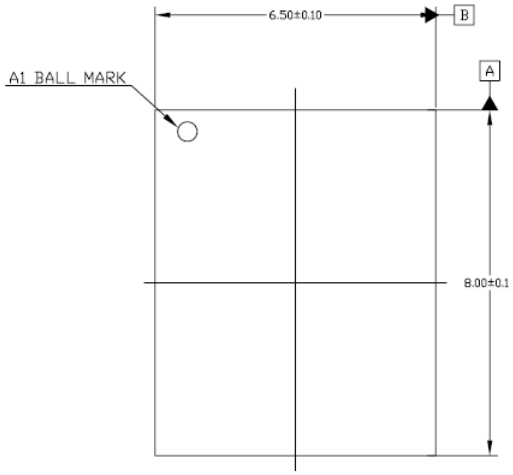


SIDE VIEW

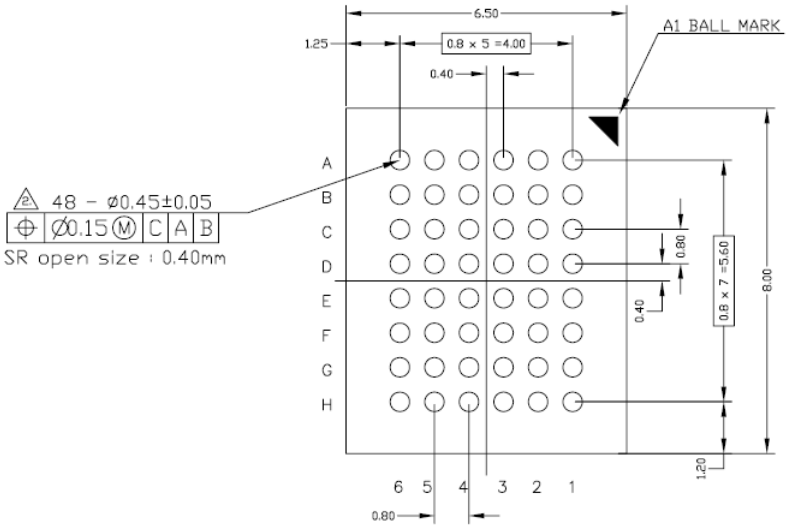
Description
FBGA 48BALL
Dimension
9.0mm x 9.0mm x 0.90mm (Max. 1.0mm T)

1. **ALL DIMENSIONS are in Millimeters.**
2. **POST REFLOW SOLDER BALL DIAMETER.**
   (Pre Reflow diameter : Ø0.40±0.02)

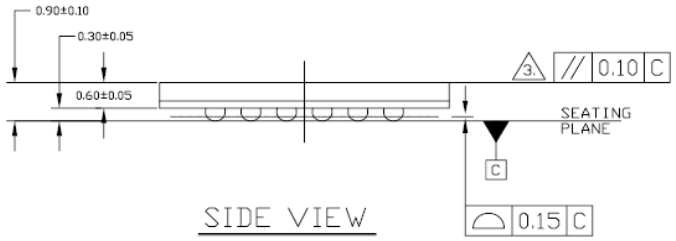
PACKAGE OUTLINE DRAWING (48ball-FBGA 6.5x8mm)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Description
FBGA 48BALL
Dimension
6.5mm x 8.0mm x 0.90mm (Max. 1.0mm T)

1. **ALL DIMENSIONS are in Millimeters.**
2. **POST REFLOW SOLDER BALL DIAMETER.**
   (Pre Reflow diameter : Ø0.40±0.02)

PIN DESCRIPTION

Pin Name	Pin Function
I/O0 ~ I/O7	DATA INPUTS/OUTPUTS The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	COMMAND LATCH ENABLE The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the /WE signal.
ALE	ADDRESS LATCH ENABLE The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of /WE with ALE high
/CE	CHIP ENABLE The /CE input is the device selection control. When the device is in the Busy state, /CE high is ignored, and the device does not return to standby mode in program or erase operation. Regarding /CE control during read operation, refer to 'Page Read' section of device operation.
/RE	READ ENABLE The /RE input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of /RE which also increments the internal column address counter by one.
/WE	WRITE ENABLE The /WE input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the /WE pulse.
/WP	WRITE PROTECT The /WP pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the /WP pin is active low.
R/B	READY/BUSY OUTPUT The R/B output indicates the status of the device operation. When low, it indicates that a program, erase of random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
VCC	POWER VCC is the power supply for device.
VSS	GROUND
N.C	NO CONNECTION Lead is not internally connected.

Note : Connect all Vcc and Vss pins of each device to common power supply outputs
Do not leave Vcc or Vss disconnected.

Figure 1. AFND1G08U3 FUNCTIONAL BLOCK DIAGRAM

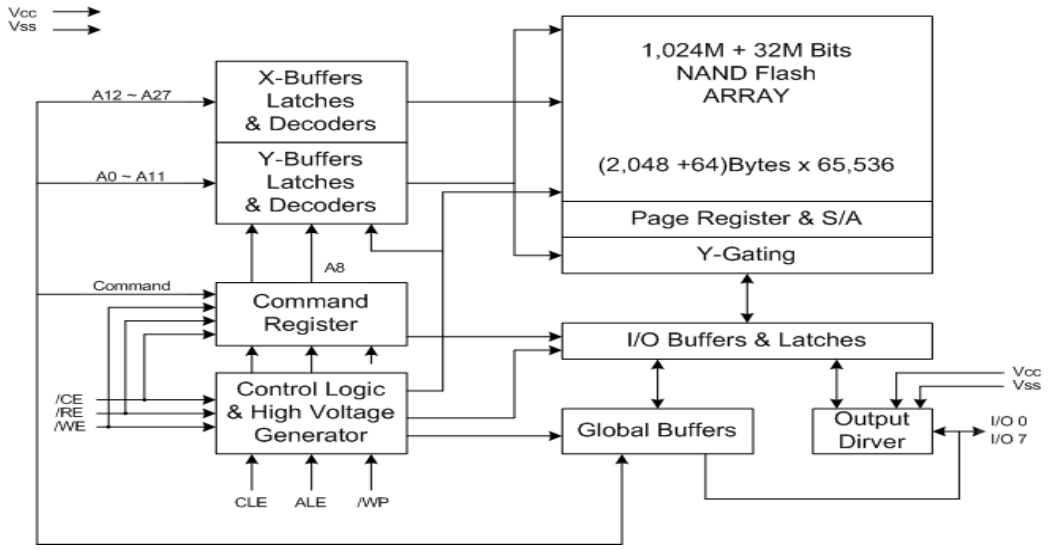
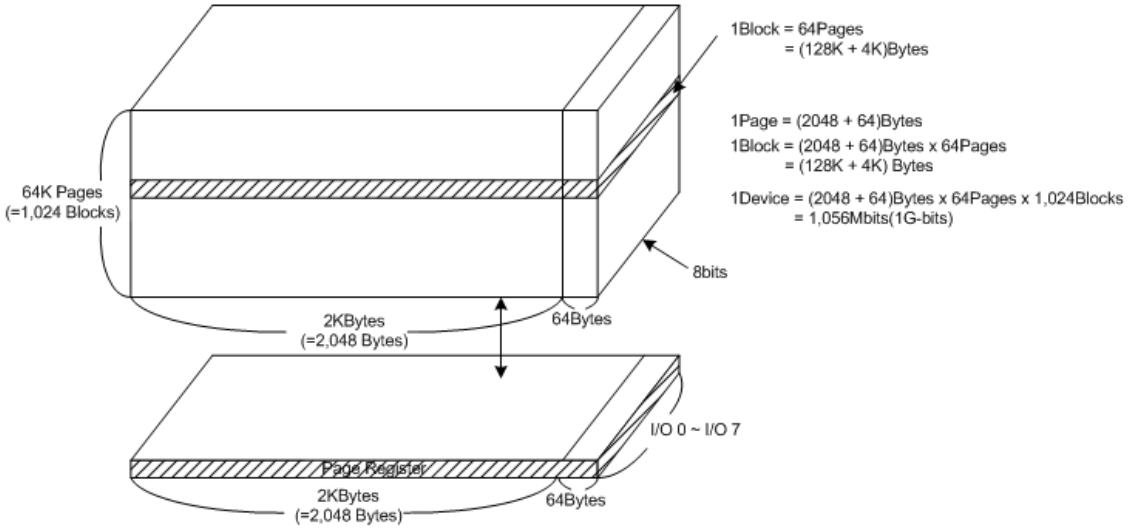


Figure 2. AFND1G08U3 ARRAY ORGANIZATION



	I/O 0	I/O 0	I/O 0	I/O 0	I/O 0	I/O 0	I/O 0	I/O 0	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	← Column Address
2nd Cycle	A8	A9	A10	A11	*L	*L	*L	*L	← Column Address
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19	← Row Address
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27	← (Page Address)

NOTE : Column Address : Starting Address of the Register.

*** L must be set to "Low"**

*** The device ignores any additional input of address cycles than required.**